RX634 Group
Renesas MCUs

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54 MHz 32-bit RX MCU with FPU, 90 DMIPS, up to 2-Mbyte flash memory, 12-bit ADC, 10-bit DAC, ELC, MPC, CEC transmission/reception, remote control signal reception

Features

■ 32-bit RX CPU core

- Max. operating frequency: 54 MHz
  Capable of 90 DMIPS in operation at 54 MHz
- Two types of multiply-and-accumulation unit (between memories and between registers)
- 32-bit multiplier (fastest instruction execution takes one CPU clock cycle)
- Divider (fastest instruction execution takes two CPU clock cycles)
- Fast interrupt
- CISC Harvard architecture with 5-stage pipeline
- Variable-length instructions, ultra-compact code
- Supports the Memory Protection Unit (MPU)
- On-chip debugging circuit

■ Low power design and architecture

- Operation from a single 2.7 to 3.6 V or 4.0 to 5.5 V supply
- Four low power consumption modes

■ On-chip main flash memory, no wait states

- 54-MHz operation, 18.5-ns read cycle
- 1 to 2 Mbytes supported
- User code is programmable by on-board

■ On-chip data flash memory

- 32 Kbytes capacities
  (Number of times of reprogramming: 100,000)
- Programming/erasing as background operations (BGOs)

■ On-chip SRAM, no wait states

- 128-Kbyte size capacities
- For instructions and operands

■ DMA

- DMAC: Incorporates four channels
- DTC

■ ELC

- Module operation can be initiated by event signals without going through interrupts.
- Modules can operate while the CPU is sleeping.

■ Reset and supply management

- Power-on reset (POR)
- Low voltage detection (LVD) with voltage settings

■ Clock functions

- External crystal oscillator or internal PLL for operation at 8 to 20 MHz
- Internal 125-kHz LOCO
- Dedicated 125-kHz LOCO for the IWDT
- Clock frequency accuracy measurement circuit (CAC)

■ Independent watchdog timer

- 125-kHz on-chip oscillator produces a dedicated clock signal to drive IWDT operation.

■ Useful functions for IEC60730 compliance

- Oscillation-stoppage detection, frequency measurement, CRC, IWDT, self-diagnostic function for the A/D converter, etc.

PLQP0144KA-A 20 × 20 mm, 0.5-mm pitch

■ Various communications interfaces

- SCI with many useful functions (up to 13 channels)
  Asynchronous mode, clock synchronous mode, smart card interface, simplified SPI, simplified I^2C, and extended serial mode
- I^2C bus interface: Transfer at up to 400 kbps (three channels)
- RSPI for high-speed transfer (two channels)

■ CEC transmission/reception function

- CEC signals can be transmitted/received conforming to CEC standard 1.4

■ Remote control signal reception

- Two units integrated
- Four pattern waveform matching supported

■ External address space

- Buses for high-speed data transfer (max. operating frequency of 27 MHz)
- 4 CS areas (4 × 16 Mbytes)
- Multiplexed bus or separate bus are selectable per area.
- 8-, or 16-bit bus space is selectable per area

■ Up to 20 extended-function timers

- 16-bit MTU: input capture, output compare, complementary PWM output, phase counting mode
  (six channels)
- 16-bit TPU: input capture, output capture, phase counting mode (six channels)
- 8-bit TMR (four channels)
- 16-bit compare-match timers (four channels)

■ 12-bit A/D converter

- Capable of conversion within 1 µs
- Sample-and-hold circuits (for three channels)
- Three-channel synchronized sampling available
- Self-diagnostic function and analog input disconnection detection assistance function

■ 10-bit D/A converter: 2 channels

■ Register write protection can protect values in important registers against overwriting

■ Up to 114 pins for general I/O ports

- Open drain, input pull-up

■ MPC

- Multiple locations are selectable for I/O pins of peripheral functions

■ Operating temperature range

- –40 to +85°C

1.Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline.

Table 1.1 Outline of Specifications (1 / 4)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 54 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register General purpose: Sixteen 32-bit registers Control: Nine 32-bit registers Accumulator: One 64-bit register • Basic instructions: 73 • Floating-point instructions: 8 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • Memory-protection unit (MPU)
	FPU	• Single precision (32-bit) floating point • Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	ROM	• Capacity: 1 M/1.5 M/2 Mbytes • 54 MHz, no-wait memory access • On-board programming: 3 types Off-board programming
	RAM	• Capacity: 128 Kbytes • 54 MHz, no-wait memory access
	E2 DataFlash	• Capacity: 32 Kbytes • Number of times for programming/erasing: 100,000
MCU operating mode		Single-chip mode, on-chip ROM enabled expansion mode, and on-chip ROM disabled expansion mode (software switching)
Clock	Clock generation circuit	• Main clock oscillator, low-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator • Oscillation stop detection • Measuring circuit for accuracy of clock frequency (clock-accuracy check: CAC) • Independent settings for the system clock (ICLK), peripheral module clock (PCLKB), external bus clock (BCLK), and FlashIF clock (FCLK) The CPU and system sections such as other bus masters run in synchronization with the system clock (ICLK): 54 MHz (at max.) Peripheral modules run in synchronization with the peripheral module clock (PCLKB): 32 MHz (at max.) Devices connected to the external bus run in synchronization with the external bus clock (BCLK): 27 MHz (at max.) The flash peripheral circuit runs in synchronization with the FlashIF clock (FCLK): 32 MHz (at max.)
Reset		RES# pin reset, power-on reset, voltage monitoring reset, watchdog timer reset, independent watchdog timer reset, deep software standby reset, and software reset
Voltage detection	Voltage detection circuit	• When the voltage on VCC falls below the voltage detection level, an internal reset or internal interrupt is generated. The detection voltage level of voltage detection circuit 0 is fixed Voltage detection circuit 1 is capable of selecting the detection voltage from 3 levels Voltage detection circuit 2 is capable of selecting the detection voltage from 3 levels
Low power consumption	Low power consumption facilities	• Module stop function • Four low power consumption modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode
	Function for lower operating power consumption	• Operating power control modes High-speed operating mode, low-speed operating mode 1, low-speed operating mode 2
Interrupt	Interrupt controller (ICUb)	• Interrupt vectors: 178 • External interrupts: 14 (NMI, IRQ0 to IRQ12 pins) • Non-maskable interrupts: 6 (the NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, WDT interrupt, and IWDT interrupt) • 16 levels specifiable for the order of priority

Table 1.1 Outline of Specifications (2 / 4)

Classification	Module/Function	Description
External bus extension		• The external address space can be divided into four areas (CS0 to CS3), each with independent control of access settings. Capacity of each area: 16 Mbytes (CS0 to CS3) A chip-select signal (CS0# to CS3#) can be output for each area. Each area is specifiable as an 8-bit or 16-bit bus space The data arrangement in each area is selectable as little or big endian (only for data). Bus format: Separate bus, multiplex bus • Wait control • Write buffer facility
DMA	DMA controller (DMACA)	• 4 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	Data transfer controller (DTCa)	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Interrupts • Chain transfer function
I/O ports	General I/O ports	144-pin • I/O: 114 • Input: 9 (P40 to P47, P35) • Pull-up resistors: 111 • Open-drain outputs: 114 • 5-V tolerance: Not supported
Event link controller (ELC)		• Event signals of 56 types can be directly connected to the module • Operations of timer modules are selectable at event input • Capable of event link operation for ports B and E
Multi-function pin controller (MPC)		• Capable of selecting input/output function from multiple pins
Timers	16-bit timer pulse unit (TPUa)	• (16 bits × 6 channels) × 1 unit • Maximum of 16 pulse-input/output possible • Select from among seven or eight counter-input clock signals for each channel • Supports the input capture/output compare function • Output of PWM waveforms in up to 15 phases in PWM mode • Support for buffered operation, phase-counting mode (two-phase encoder input) and cascade-connected operation (32 bits × 2 channels) depending on the channel. • Capable of generating conversion start triggers for the A/D converters • Signals from the input capture pins are input via a digital filter
	Multi-function timer pulse unit 2 (MTU2a)	• (16 bits × 6 channels) × 1 unit • Up to 16 pulse-input/output lines and three pulse-input lines are available with six 16-bit timer channels • Select from among eight or seven counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. • Input capture function • 21 output compare/input capture registers • Pulse output mode • Complementary PWM output mode • Reset synchronous PWM mode • Phase-counting mode • Generation of triggers for A/D converter conversion
	Port output enable 2 (POE2a)	Controls the high-impedance state of the MTU's waveform output pins
	Programmable pulse generator (PPG)	• (4 bits × 4 groups) × 1 unit • Pulse output with the MTU output as a trigger • Maximum of 16 pulse-output possible
	8-bit timer (TMR)	• (8 bits × 2 channels) × 2 units • Select from among seven internal clock signals (PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192) and one external clock signal • Capable of output of pulse trains with desired duty cycles or of PWM signals • The 2 channels of each unit can be cascaded to create a 16-bit timer • Capable of generating baud-rate clocks for SCI5, SCI6, and SCI12 • Capable of generating a receive clock for the RCR
	Compare match timer (CMT)	• (16 bits × 2 channels) × 2 units • Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Watchdog timer (WDTA)	• 14 bits × 1 channel • Select from among six counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192)

Table 1.1 Outline of Specifications (3 / 4)

Classification	Module/Function	Description
Timers	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Counter-input clock: IWDT-dedicated on-chip oscillator Frequency divided by 1, 16, 32, 64, 128, or 256
Communication functions	Serial communications interfaces (SCIe, SCIf)	• 13 channels (channel 0 to 11: SCIe, channel 12: SCIf) • Serial communications modes: Asynchronous, clock synchronous, and smart-card interface • On-chip baud rate generator allows selection of the desired bit rate • Choice of LSB-first or MSB-first transfer • Average transfer rate clock can be input from TMR timers (SCI5, SCI6, and SCI12) • Simple IIC • Simple SPI • Master/slave mode supported (SCIf only) • Start frame and information frame are included (SCIf only)
	I²C bus interface (RIIC)	• 3 channel • Communications formats: I²C bus format/SMBus format • Master/slave selectable • Max. transfer rate: Supports the fast mode (400 Kbps)
	Serial peripheral interface (RSPI)	• 2 channels • Transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPI clock (RSPCK) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) • Capable of handling serial transfer as a master or slave • Data formats Choice of LSB-first or MSB-first transfer The number of bits in each transfer can be changed to any number of bits from 8 to 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Double buffers for both transmission and reception
	CEC transmission/ reception circuit (CEC) (3-V packages only)	CEC signals can be generated and received conforming to the CEC standard, and communication states can be detected by hardware. • Serial communication can be performed conforming to the CEC standard. • The operating clock can be selected from among the PCLK, main clock, and IWDTCLK. • Any value can be set for the low-level width/bit width of the start bit and data bit during transmission and reception. • Errors and communication states can be detected by hardware. • An error handling pulse can be output when a timing error of the long bit width is detected. • Signal-free time can be counted. • Receive operation can be restarted by detecting the start bit during reception.
	Remote control signal receiver (RCR) (3-V packages only)	• Two units • Four pattern matching (header, data 0, data 1, and special data detection) • 8-byte receive buffer per unit • The operating clock can be selected from among the PCLK, main clock, IWDTCLK, and TMR.
12-bit A/D converter (S12ADb)		• 12 bits (16 channels × 1 unit) • 12-bit resolution • Minimum conversion time: 1.0 μs per channel (in operation with ADCLK at 50 MHz) • Operating modes Scan mode (single scan mode, continuous scan mode, and group scan mode) • Sample-and-hold function • Self-diagnosis for the A/D converter • Assistance in detecting disconnected analog inputs • Double-trigger mode (duplication of A/D conversion data) • A/D conversion start conditions A software trigger, a trigger from a timer (MTU), an external trigger signal, or ELC
D/A converter (DA)		• 2 channels • 10-bit resolution • Output voltage: 0 V to VREFH
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Data Operation Circuit (DOC)		Comparison, addition, and subtraction of 16-bit data
Operating frequency		54 MHz

Table 1.1 Outline of Specifications (4 / 4)

Classification	Module/Function	Description
Power supply voltage		• 3-V package VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V • 5-V package VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V
Operating temperature		–40 to +85°C (products with wide-temperature-range spec.)
Packages		144-pin LQFP (PLQP0144KA-A)
On-chip debugging system		• E1 emulator (JTAG and FINE interfaces) • E20 emulator (JTAG interface)

Table 1.2 Comparison of Functions of Different RX634 Group Products

Functions		**RX634 Group**	
Group Products		**3-V package**	**5-V package**
External bus	External bus width	16 bits	
DMA	DMA controller	Channels 0 to 3	
	Data transfer controller	Supported	
Timers	16-bit timer pulse unit	Channels 0 to 5	
	Multi-function timer pulse unit 2	Channels 0 to 5	
	Port output enable 2	Supported	
	Programmable pulse generator	Supported	
	8-bit timer	Channels 0 to 3	
	Compare match timer	Channels 0 to 3	
	Watchdog timer	Supported	
	Independent watchdog timer	Supported	
Communication functions	Serial communications interface (SCIe)	Channels 0 to 11	
	Serial communications interface (SCIf)	Channel 12	
	I^2C bus interface	Channels 0, 1, 3	
	Serial peripheral interface	Channels 0, 1	
	CEC transmission/reception circuit (CEC)	Supported	Not supported
	Remote control signal receiver (RCR)	Channels 0, 1	Not supported
12-bit A/D converter		AN000 to AN015	
D/A converter		Channels 0, 1	
CRC calculator		Supported	
Event link controller		Supported	
Clock frequency accuracy measurement circuit (CAC)		Supported	

1.2 List of Products

Table 1.3 is a lists of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products

Group	Part No.	Orderable Part No.	Package	ROM Capacity	RAM Capacity	Power Supply Voltage
RX634	R5F5634EYDFB	R5F5634EYDFB#30	PLQP0144KA-A	2 Mbytes	128 Kbytes	VCC = AVCC0 = 4.0 to 5.5V
	R5F5634ECDFB	R5F5634ECDFB#30	PLQP0144KA-A	2 Mbytes	128 Kbytes	VCC = AVCC0 = 2.7 to 3.6V
	R5F5634DYDFB	R5F5634DYDFB#30	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	VCC = AVCC0 = 4.0 to 5.5V
	R5F5634DCDFB	R5F5634DCDFB#30	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	VCC = AVCC0 = 2.7 to 3.6V
	R5F5634BYDFB	R5F5634BYDFB#30	PLQP0144KA-A	1 Mbyte	128 Kbytes	VCC = AVCC0 = 4.0 to 5.5V
	R5F5634BCDFB	R5F5634BCDFB#30	PLQP0144KA-A	1 Mbyte	128 Kbytes	VCC = AVCC0 = 2.7 to 3.6V

Note: Orderable part numbers are current as of when this manual was published. Please make sure to refer to the relevant product page on the Renesas website for the latest part numbers.

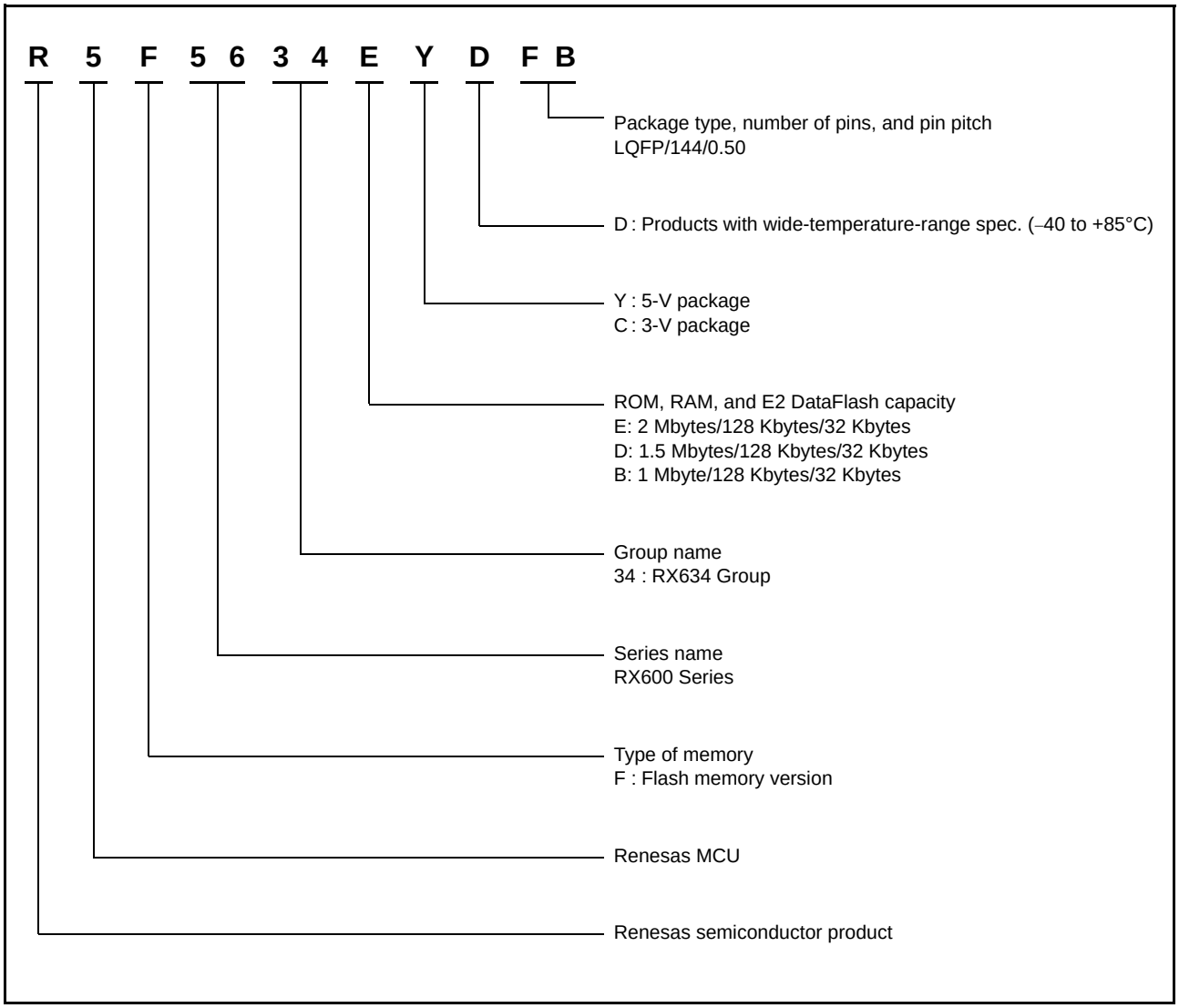
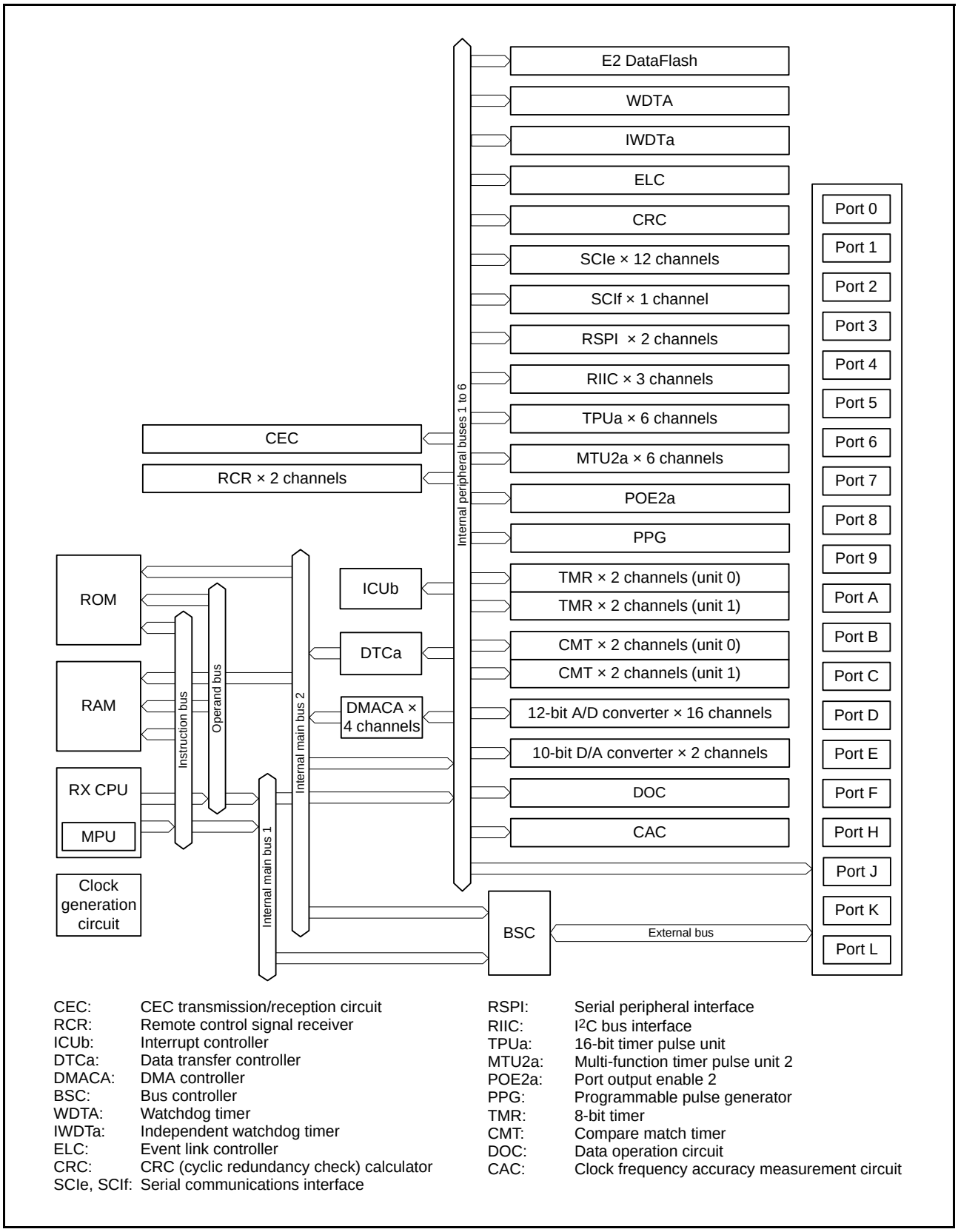


Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type

1.3 Block Diagram

Figure 1.2 shows a block diagram.



CEC: CEC transmission/reception circuit
RCR: Remote control signal receiver
ICUb: Interrupt controller
DTCa: Data transfer controller
DMACA: DMA controller
BSC: Bus controller
WDTA: Watchdog timer
IWDTa: Independent watchdog timer
ELC: Event link controller
CRC: CRC (cyclic redundancy check) calculator
SCIe, SCIf: Serial communications interface
RSPI: Serial peripheral interface
RIIC: I^2C bus interface
TPUa: 16-bit timer pulse unit
MTU2a: Multi-function timer pulse unit 2
POE2a: Port output enable 2
PPG: Programmable pulse generator
TMR: 8-bit timer
CMT: Compare match timer
DOC: Data operation circuit
CAC: Clock frequency accuracy measurement circuit

Figure 1.2 Block Diagram

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1 / 4)

Classifications	Pin Name	I/O	Description
Power supply	VCC	—	Power supply pin. Connect this pin to the system power supply. Connect the pin to VSS via a 0.1-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	VCL	—	Connect this pin to the VSS pin via the 0.1 μF smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	—	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for connecting a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	BCLK	Output	Outputs the external bus clock for external devices.
Clock frequency accuracy measurement	CACREF	Input	Input for the trigger signal in measuring accuracy of the clock frequency
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on this pin must not be changed during operation.
System control	RES#	Input	Reset pin. This MCU enters the reset state when this signal goes low.
	EMLE	Input	Input pin for the on-chip emulator enable signal. When the onchip emulator is used, this pin should be driven high. When not used, it should be driven low.
On-chip emulator	FINEC	Input	Fine interface clock pin
	FINED	I/O	Fine interface pin
	TRST#	Input	On-chip emulator pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator.
	TMS	Input	
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TRCLK	Output	This pin outputs the clock for synchronization with the trace data.
	TRSYNC#	Output	This pin indicates that output from the TRDATA0 to TRDATA3 pins is valid.
	TRDATA0 to TRDATA3	Output	These pins output the trace information.
Address bus	A0 to A23	Output	Output pins for the address.
Data bus	D0 to D15	I/O	Input and output pins for the bidirectional data bus.
Multiplexed bus	A0/D0 to A15/D15	I/O	Address/data multiplexed bus
Bus control	RD#	Output	Strobe signal which indicates that reading from the external bus interface space is in progress.
	WR#	Output	Strobe signal which indicates that writing to the external bus interface space is in progress, in single-write strobe mode.
	WR0# to WR1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, and D15 to D8) is valid in writing to the external bus interface space, in byte strobe mode.
	BC0# to BC1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0 and D15 to D8) is valid in access to the external bus interface space, in single-write strobe mode.
	ALE	Output	Address latch signal when address/data multiplexed bus is selected.
	WAIT#	Input	Input pin for wait request signals in access to the external space.
	CS0# to CS3#	Output	Select signals for areas 0 to 3.

Table 1.4 Pin Functions (2 / 4)

Classifications	Pin Name	I/O	Description
Interrupt	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ12	Input	Interrupt request pins.
16-bit timer pulse unit	TIOCA0, TIOCB0 TIOCC0, TIOCD0	I/O	The TGRA0 to TGRD0 input capture input/output compare output/ PWM output pins.
	TIOCA1, TIOCB1	I/O	The TGRA1 and TGRB1 input capture input/output compare output/ PWM output pins.
	TIOCA2, TIOCB2	I/O	The TGRA2 and TGRB2 input capture input/output compare output/ PWM output pins.
	TIOCA3, TIOCB3 TIOCC3, TIOCD3	I/O	The TGRA3 to TGRD3 input capture input/output compare output/ PWM output pins.
	TIOCA4, TIOCB4	I/O	The TGRA4 and TGRB4 input capture input/output compare output/ PWM output pins.
	TIOCA5, TIOCB5	I/O	The TGRA5 and TGRB5 input capture input/output compare output/ PWM output pins.
	TCLKA, TCLKB TCLKC, TCLKD	Input	Input pins for external clock signals.
Multi-function timer pulse unit 2	MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/ PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/ PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/ PWM output pins.
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/ PWM output pins.
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/ PWM output pins.
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for the external clock.
Port output enable 2	POE0# to POE3#, POE8#	Input	Input pins for request signals to place the MTU pins in the high impedance state.
Programmable pulse generator	PO0 to PO15	Output	Output pins for the pulse signals.
8-bit timer	TMO0 to TMO3	Output	Compare match output pins.
	TMCI0 to TMCI3	Input	Input pins for external clocks to be input to the counter.
	TMRI0 to TMRI3	Input	Input pins for the counter reset.

Table 1.4 Pin Functions (3 / 4)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIe)	• Asynchronous mode/clock synchronous mode		
	SCK0 to SCK11	I/O	Input/output pins for the clock
	RXD0 to RXD11	Input	Input pins for received data
	TXD0 to TXD11	Output	Output pins for transmitted data
	CTS0# to CTS11#	Input	Input pins for controlling the start of transmission and reception
	RTS0# to RTS11#	Output	Output pins for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL0 to SSCL11	I/O	Input/output pins for the I^2C clock
	SSDA0 to SSDA11	I/O	Input/output pins for the I^2C data
	• Simple SPI mode		
	SCK0 to SCK11	I/O	Input/output pins for the clock
	SMISO0 to SMISO11	I/O	Input/output pins for slave transmission of data
	SMOSI0 to SMOSI11	I/O	Input/output pins for master transmission of data
	SS0# to SS11#	Input	Chip-select input pins
Serial communications interface (SCIf)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock
	RXD12	Input	Input pin for received data
	TXD12	Output	Output pin for transmitted data
	CTS12#	Input	Input pin for controlling the start of transmission and reception
	RTS12#	Output	Output pin for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL12	I/O	Input/output pin for the I^2C clock
	SSDA12	I/O	Input/output pin for the I^2C data
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock
	SMISO12	I/O	Input/output pin for slave transmit data
	SMOSI12	I/O	Input/output pin for master transmit data
	SS12#	Input	Chip-select input pin
	• Extended serial mode		
	RXDX12	Input	Input pin for data reception by SCId
	TXDX12	Output	Output pin for data transmission by SCId
	SIOX12	I/O	Input/output pin for data reception or transmission by SCId
I^2C bus interface	SCL0, SCL1, SCL3	I/O	Input/output pin for I^2C bus interface clocks. Bus can be directly driven by the N-channel open-drain output.
	SDA0, SDA1, SDA3	I/O	Input/output pin for I^2C bus interface data. Bus can be directly driven by the N-channel open-drain output.
Serial peripheral interface	RSPCKA, RSPCKB	I/O	Clock input/output pin for the RSPI.
	MOSIA, MOSIB	I/O	Input or output data output from the master for the RSPI.
	MISOA, MISOB	I/O	Input or output data output from the slave for the RSPI.
	SSLA0, SSLB0	I/O	Input/output pin to select the slave for the RSPI.
	SSLA1 to SSLA3 SSLB1 to SSLB3	Output	Output pins to select the slave for the RSPI.
CEC transmission/ reception circuit (CEC)	CECIO	I/O	Input/output pin for CEC communication data
Remote control signal receiver (RCR)	PMC0	Input	Input pin for external pulse signal
	PMC1	Input	Input pin for external pulse signal

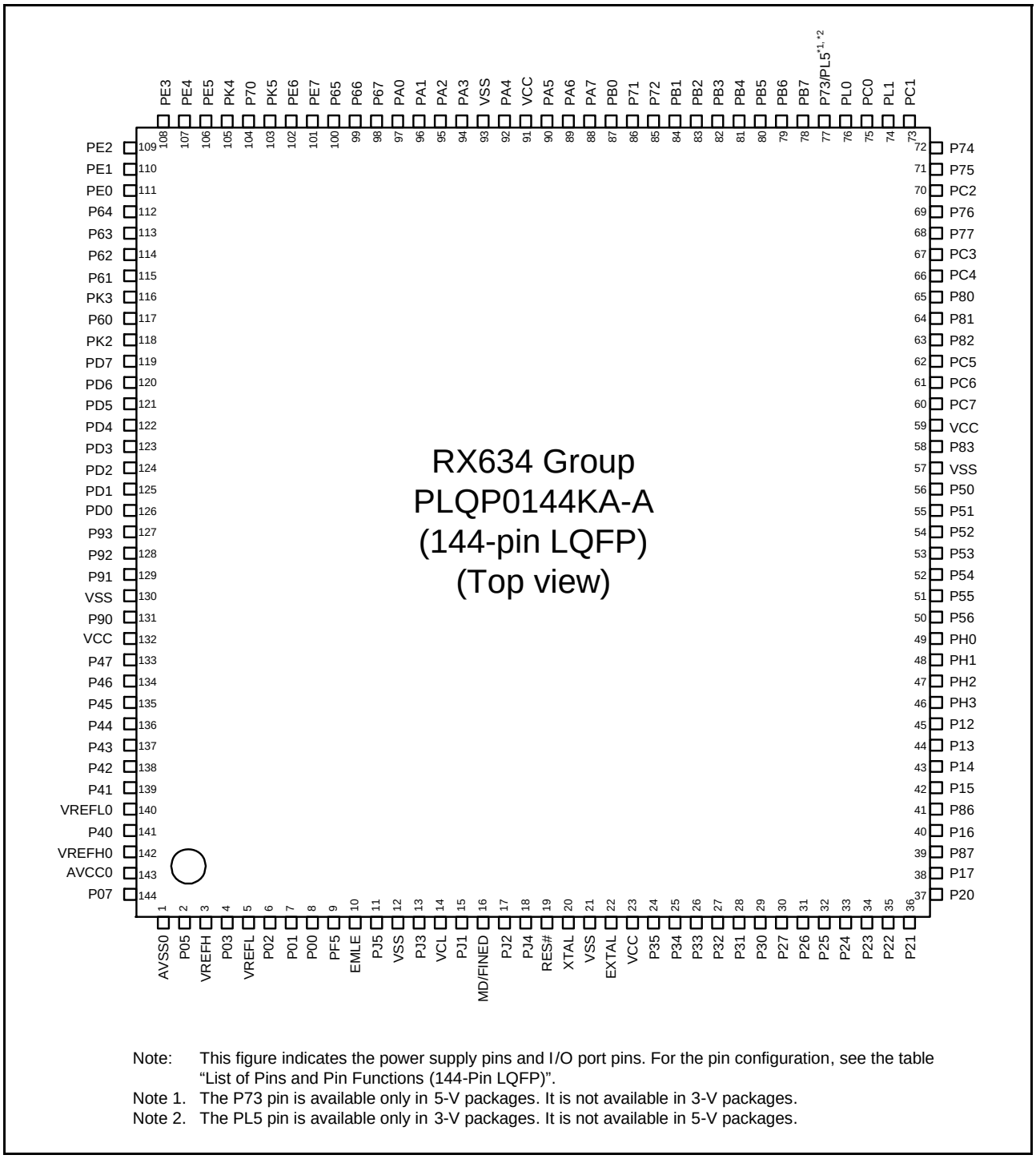
Table 1.4 Pin Functions (4 / 4)

Classifications	Pin Name	I/O	Description
12-bit A/D converter	AN000 to AN015	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0#	Input	Input pin for the external trigger signals that start the A/D conversion.
D/A converter	DA0, DA1	Output	Output pins for the analog signals to be processed by the D/A converter.
Analog power supply	AVCC0	—	Analog voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	AVSS0	—	Analog ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used.
	VREFH0	—	Analog reference voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	VREFL0	—	Analog reference ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used.
	VREFH	—	Analog voltage supply pin for the D/A converter. Connect this pin to VCC if the D/A converter is not to be used.
	VREFL	—	Analog ground pin for the D/A converter. Connect this pin to VSS if the D/A converter is not to be used.
I/O ports	P00 to P03, P05, P07	I/O	6-bit input/output pins.
	P12 to P17	I/O	6-bit input/output pins.
	P20 to P27	I/O	8-bit input/output pins.
	P30 to P35	I/O	6-bit input/output pins. (P35 input pin)
	P40 to P47	Input	8-bit input pins.
	P50 to P56	I/O	7-bit input/output pins.
	P60 to P67	I/O	8-bit input/output pins.
	P70 to P77*1	I/O	8-bit input/output pins.
	P80 to P83, P86, P87	I/O	6-bit input/output pins.
	P90 to P93	I/O	4-bit input/output pins.
	PA0 to PA7	I/O	8-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PC0 to PC7	I/O	8-bit input/output pins.
	PD0 to PD7	I/O	8-bit input/output pins.
	PE0 to PE7	I/O	8-bit input/output pins.
	PF5	I/O	1-bit input/output pin.
	PH0 to PH3	I/O	4-bit input/output pins.
	PJ1 to PJ5	I/O	5-bit input/output pins.
	PK2 to PK5	I/O	4-bit input/output pins.
	PL0, PL1, PL5*2	I/O	3-bit input/output pins.

Note 1. The P73 pin is available only in 5-V packages. It is not available in 3-V packages.
Note 2. The PL5 pin is available only in 3-V packages. It is not available in 5-V packages.

1.5 Pin Assignments

Figure 1.3 shows the pin assignments. Table 1.5 shows the lists of pins and pin functions.



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table "List of Pins and Pin Functions (144-Pin LQFP)".
Note 1. The P73 pin is available only in 5-V packages. It is not available in 3-V packages.
Note 2. The PL5 pin is available only in 3-V packages. It is not available in 5-V packages.

Figure 1.3 Pin Assignments of the 144-Pin LQFP

Table 1.5 List of Pins and Pin Functions (144-Pin LQFP) (1 / 4)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TPU, TMR, POE, PPG, CAC)	Communications (SCIe, SCIf, RSPI, RIIC, CEC, RCR)	Interrupt	AD, DA
1	AVSS0						
2		P05					DA1
3	VREFH						
4		P03				IRQ11	DA0
5	VREFL						
6		P02		TMCI1	SCK6	IRQ10	
7		P01		TMCI0	RXD6/SMISO6/SSCL6/PMC1	IRQ9	
8		P00		TMRI0	TXD6/SMOSI6/SSDA6/PMC0	IRQ8	
9		PF5				IRQ4	
10	EMLE						
11		PJ5					
12	VSS						
13		PJ3		MTIOC3C	CTS0#/RTS0#/SS0#/CTS6#/ RTS6#/SS6#		
14	VCL						
15		PJ1		MTIOC3A			
16	MD/FINED						
17		PJ2					
18		PJ4					
19	RES#						
20	XTAL						
21	VSS						
22	EXTAL						
23	VCC						
24		P35				NMI	
25	TRST#	P34		MTIOC0A/TMCI3/POE2#/ PO12	SCK0/SCK6	IRQ4	
26		P33		MTIOC0D/TIOCD0/TMRI3/ POE3#/PO11	RXD0/SMISO0/SSCL0/RXD6/ SMISO6/SSCL6	IRQ3_DS	
27		P32		MTIOC0C/TIOCC0/TMO3/ PO10	TXD0/SMOSI0/SSDA0/TXD6/ SMOSI6/SSDA6	IRQ2_DS	
28	TMS	P31		MTIOC4D/TMCI2/PO9	CTS1#/RTS1#/SS1#/SSLB0	IRQ1_DS	
29	TDI	P30		MTIOC4B/TMRI3/POE8#/ PO8	RXD1/SMISO1/SSCL1/MISOB	IRQ0_DS	
30	FINEC/TCK	P27	CS3#	MTIOC2B/TMCI3/PO7	SCK1/RSPCKB		
31	TDO	P26	CS2#	MTIOC2A/TMO1/PO6	TXD1/SMOSI1/SSDA1/CTS3#/ RTS3#/SS3#/MOSIB		
32		P25	CS1#	MTIOC4C/MTCLKB/TIOCA4/ PO5	RXD3/SMISO3/SSCL3		ADTRG0#
33		P24	CS0#	MTIOC4A/MTCLKA/TIOCB4/ TMRI1/PO4	SCK3		
34		P23		MTIOC3D/MTCLKD/ TIOCD3/PO3	TXD3/SMOSI3/SSDA3/CTS0#/ RTS0#/SS0#		
35		P22		MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2	SCK0		
36		P21		MTIOC1B/TIOCA3/TMCI0/ PO1	RXD0/SMISO0/SSCL0/SCL1	IRQ9	
37		P20		MTIOC1A/TIOCB3/TMRI0/ PO0	TXD0/SMOSI0/SSDA0/SDA1	IRQ8	
38		P17		MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ POE8#/PO15	SCK1/TXD3/SMOSI3/SSDA3/ MISOA/SDA0_DS	IRQ7	

Table 1.5 List of Pins and Pin Functions (144-Pin LQFP) (2 / 4)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TPU, TMR, POE, PPG, CAC)	Communications (SCIe, SCIf, RSPI, RIIC, CEC, RCR)	Interrupt	AD, DA
39		P87		TIOCA2			
40		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/PO14	TXD1/SMOSI1/SSDA1/RXD3/ SMISO3/SSCL3/MOSIA/ SCL0_DS	IRQ6	ADTRG0#
41		P86		TIOCA0			
42		P15		MTIOC0B/MTCLKB/TIOCB2/ TCLKB/TMCI2/PO13	RXD1/SMISO1/SSCL1/SCK3	IRQ5	
43		P14		MTIOC3A/MTCLKA/TIOCB5/ TCLKA/TMRI2/PO15	CTS1#/RTS1#/SS1#	IRQ4	
44		P13		MTIOC0B/TIOCA5/TMO3/ PO13	TXD2/SMOSI2/SSDA2/SDA0	IRQ3	
45		P12		TMCI1	RXD2/SMISO2/SSCL2/SCL0	IRQ2	
46		PH3		TMCI0			
47		PH2		TMRI0		IRQ1	
48		PH1		TMO0		IRQ0	
49		PH0		CACREF			
50		P56		MTIOC3C/TIOCA1			
51	TRDATA3	P55	WAIT#	MTIOC4D/TMO3		IRQ10	
52	TRDATA2	P54	ALE	MTIOC4B/TMCI1	CTS2#/RTS2#/SS2#		
53		P53	BCLK				
54		P52	RD#		RXD2/SMISO2/SSCL2/SSLB3		
55		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2		
56		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2/SSLB1		
57	VSS						
58	TRCLK	P83		MTIOC4C	CTS10#/RTS10#/SS10#		
59	VCC						
60		PC7	A23/CS0#	MTIOC3A/MTCLKB/TMO2/ CACREF	TXD8/SMOSI8/SSDA8/MISOA		
61		PC6	A22/CS1#	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/MOSIA		
62		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA		
63	TRSYNC#	P82		MTIOC4A	TXD10/SMOSI10/SSDA10		
64	TRDATA1	P81		MTIOC3D	RXD10/SMISO10/SSCL10		
65	TRDATA0	P80		MTIOC3B	SCK10		
66		PC4	A20/CS3#	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/RTS8#/SS8#/ SSLA0		
67		PC3	A19	MTIOC4D/TCLKB	TXD5/SMOSI5/SSDA5		
68		P77			TXD11/SMOSI11/SSDA11		
69		P76			RXD11/SMISO11/SSCL11		
70		PC2	A18	MTIOC4B/TCLKA	RXD5/SMISO5/SSCL5/SSLA3		
71		P75			SCK11		
72		P74			CTS11#/RTS11#/SS11#		
73		PC1	A17	MTIOC3A/TCLKD	SCK5/SSLA2/SDA3	IRQ12	
74		PL1					
75		PC0	A16	MTIOC3C/TCLKC	CTS5#/RTS5#/SS5#/SSLA1/ SCL3		
76		PL0					
77		P73*1				IRQ12	
		PL5*1			CECIO	IRQ12	
78		PB7	A15	MTIOC3B/TIOCB5	TXD9/SMOSI9/SSDA9		

Table 1.5 List of Pins and Pin Functions (144-Pin LQFP) (3 / 4)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TPU, TMR, POE, PPG, CAC)	Communications (SCIe, SCIf, RSPI, RIIC, CEC, RCR)	Interrupt	AD, DA
79		PB6	A14	MTIOC3D/TIOCA5	RXD9/SMISO9/SSCL9		
80		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/POE1#	SCK9		
81		PB4	A12	TIOCA4	CTS9#/RTS9#/SS9#		
82		PB3	A11	MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/TMO0/ POE3#	SCK4/SCK6		
83		PB2	A10	TIOCC3/TCLKC	CTS4#/RTS4#/SS4#/CTS6#/ RTS6#/SS6#		
84		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMCI0	TXD4/SMOSI4/SSDA4/TXD6/ SMOSI6/SSDA6	IRQ4_DS	
85		P72					
86		P71					
87		PB0	A8	MTIC5W/TIOCA3	RXD4/SMISO4/SSCL4/RXD6/ SMISO6/SSCL6/RSPCKA	IRQ12	
88		PA7	A7	TIOCB2	MISOA		
89		PA6	A6	MTIC5V/MTCLKB/TIOCA2/ TMCI3/POE2#	CTS5#/RTS5#/SS5#/MOSIA		
90		PA5	A5	TIOCB1	RSPCKA		
91	VCC						
92		PA4	A4	MTIC5U/MTCLKA/TIOCA1/ TMRI0	TXD5/SMOSI5/SSDA5/SSLA0	IRQ5_DS	
93	VSS						
94		PA3	A3	MTIOC0D/MTCLKD/ TIOCD0/TCLKB	RXD5/SMISO5/SSCL5	IRQ6_DS	
95		PA2	A2		RXD5/SMISO5/SSCL5/SSLA3		
96		PA1	A1	MTIOC0B/MTCLKC/TIOCB0	SCK5/SSLA2	IRQ11	
97		PA0	A0/BC0#	MTIOC4A/TIOCA0/CACREF	SSLA1		
98		P67					
99		P66					
100		P65					
101		PE7	D15 [A15/D15]		MISOB	IRQ7	AN015
102		PE6	D14 [A14/D14]		CTS4#/RTS4#/SS4#/MOSIB	IRQ6	AN014
103		PK5			TXD4/SMOSI4/SSDA4		
104		P70			SCK4		
105		PK4			RXD4/SMISO4/SSCL4		
106		PE5	D13 [A13/D13]	MTIOC4C/MTIOC2B	RSPCKB	IRQ5	AN013
107		PE4	D12 [A12/D12]	MTIOC4D/MTIOC1A	SSLB0		AN012
108		PE3	D11 [A11/D11]	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#/ MISOB		AN011
109		PE2	D10 [A10/D10]	MTIOC4A	RXD12/RXDX12/SMISO12/ SSCL12/SSLB3/MOSIB	IRQ7_DS	AN010
110		PE1	D9 [A9/D9]	MTIOC4C	TXD12/TXDX12/SMOSI12/ SSDA12/SSLB2/RSPCKB/ SIOX12		AN009
111		PE0	D8 [A8/D8]		SCK12/SSLB1		AN008
112		P64					
113		P63					
114		P62					
115		P61			CTS9#/RTS9#/SS9#		
116		PK3			RXD9/SMISO9/SSCL9		
117		P60			SCK9		

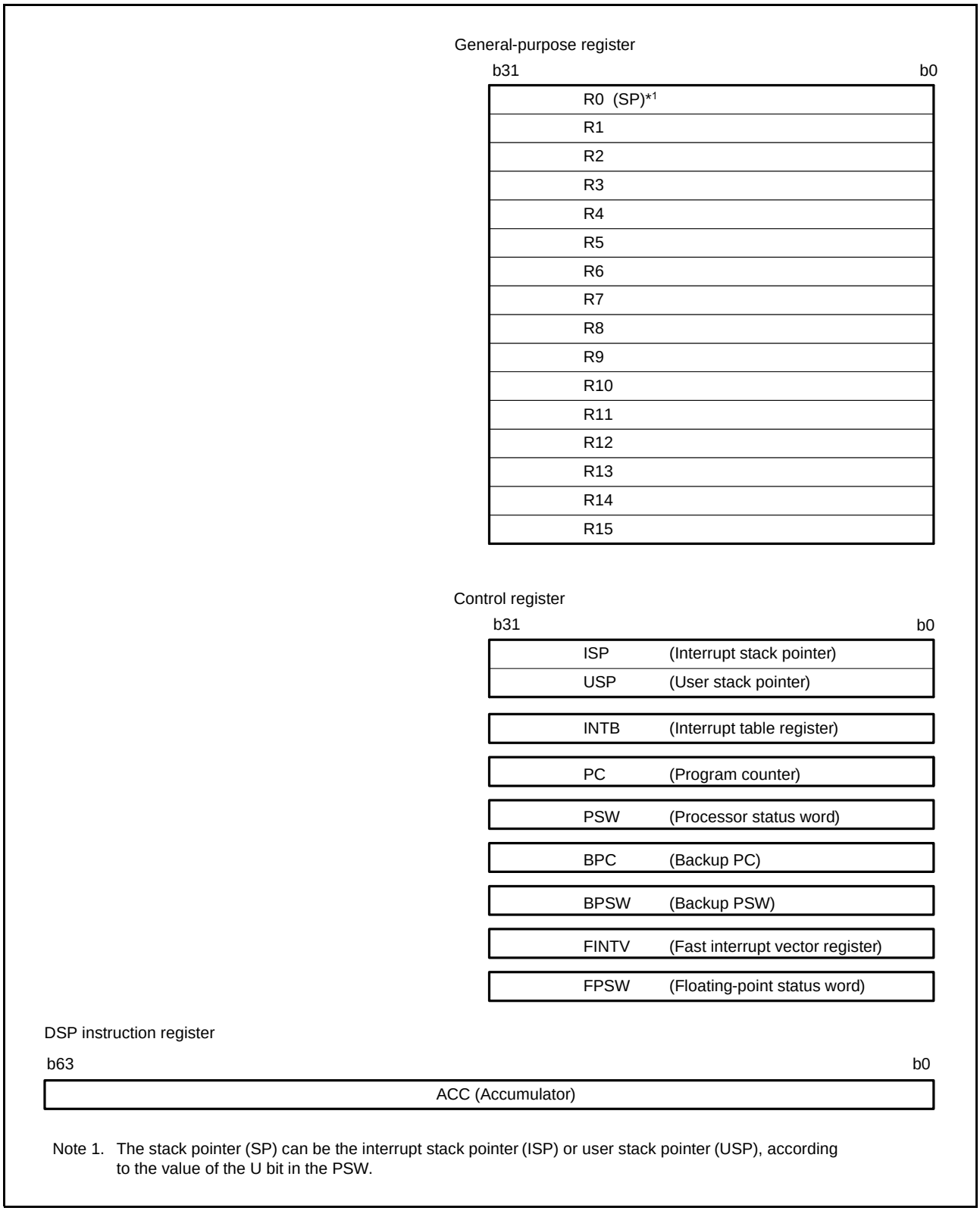
Table 1.5 List of Pins and Pin Functions (144-Pin LQFP) (4 / 4)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TPU, TMR, POE, PPG, CAC)	Communications (SCIe, SCIf, RSPI, RIIC, CEC, RCR)	Interrupt	AD, DA
118		PK2			TXD9/SMOSI9/SSDA9		
119		PD7	D7 [A7/D7]	MTIC5U/POE0#		IRQ7	
120		PD6	D6 [A6/D6]	MTIC5V/POE1#		IRQ6	
121		PD5	D5 [A5/D5]	MTIC5W/POE2#		IRQ5	
122		PD4	D4 [A4/D4]	POE3#		IRQ4	
123		PD3	D3 [A3/D3]	POE8#		IRQ3	
124		PD2	D2 [A2/D2]	MTIOC4D		IRQ2	
125		PD1	D1 [A1/D1]	MTIOC4B		IRQ1	
126		PD0	D0 [A0/D0]			IRQ0	
127		P93			CTS7#/RTS7#/SS7#		
128		P92			RXD7/SMISO7/SSCL7		
129		P91			SCK7		
130	VSS						
131		P90			TXD7/SMOSI7/SSDA7		
132	VCC						
133		P47					AN007
134		P46					AN006
135		P45					AN005
136		P44					AN004
137		P43					AN003
138		P42					AN002
139		P41					AN001
140	VREFL0						
141		P40					AN000
142	VREFH0						
143	AVCC0						
144		P07					ADTRG0#

Note 1. Pin 77 is available as P73 in 5-V packages, and PL5 in 3-V packages.

2. CPU

Figure 2.1 shows the register set of the CPU.



Note 1. The stack pointer (SP) can be the interrupt stack pointer (ISP) or user stack pointer (USP), according to the value of the U bit in the PSW.

Figure 2.1 Register Set of the CPU

2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen general-purpose registers (R0 to R15). R1 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP).
The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).
Set the ISP or USP to a multiple of four, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.

(3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(4) Processor Status Word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

(5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

(6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.
The FINTV register specifies a branch destination address when a fast interrupt has been generated.

(8) Floating-Point Status Word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.
When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).

2.3 Register Associated with DSP Instructions

(1) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.

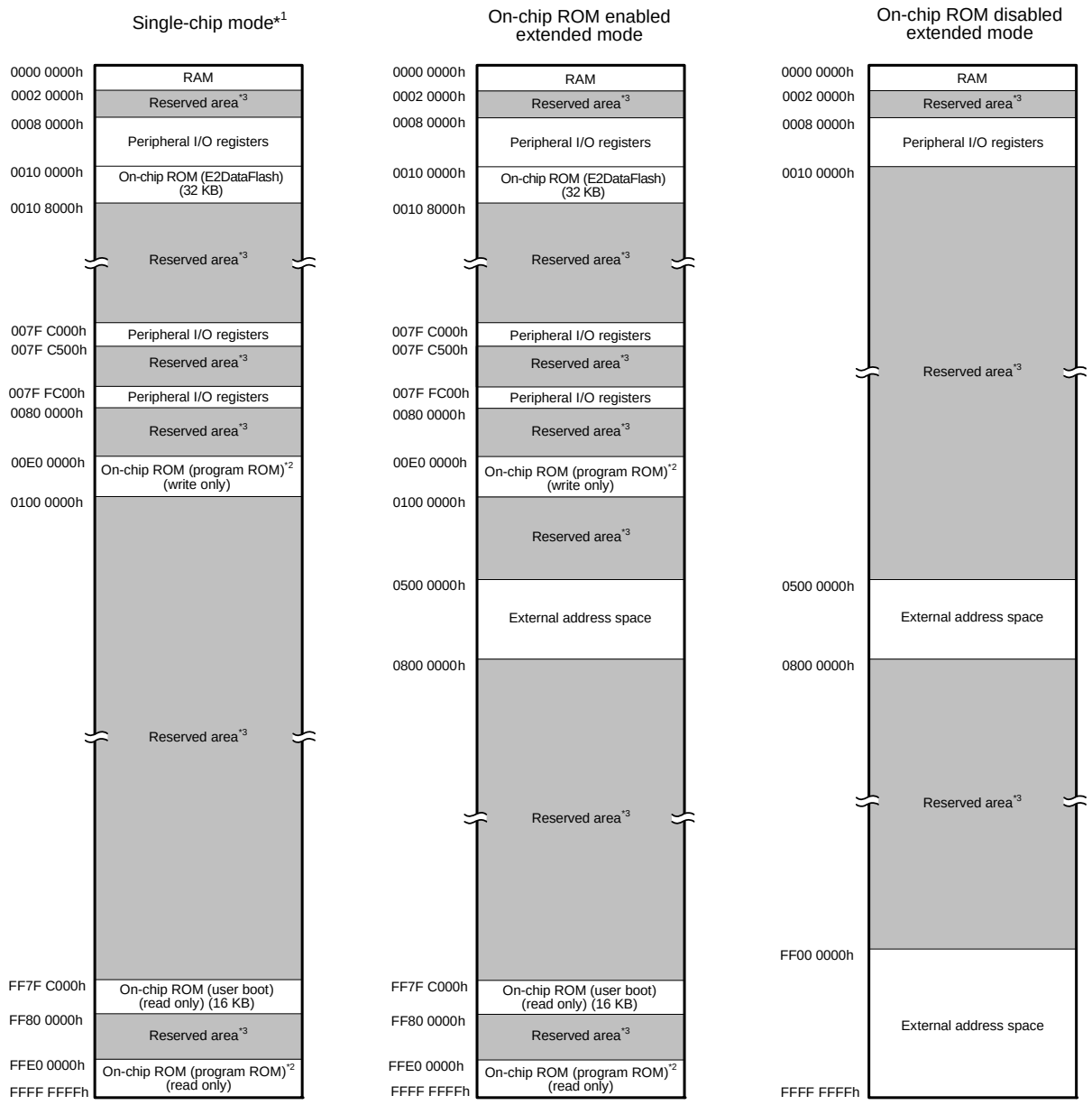
Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.

Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

3. Address Space

3.1 Address Space

This LSI has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.
Figure 3.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.



Note 1. The address space in boot mode and user boot mode is the same as the address space in single-chip mode.
Note 2. The ROM capacity differs depending on the products.

ROM (Byte)			RAM (Byte)	
Capacity	Address (for Reading)	Address (for Writing)	Capacity	Address
2 M	FFE0 0000h to FFFF FFFFh	00E0 0000h to 00FF FFFFh	128 K	0000 0000h to 0001 FFFFh
1.5 M	FFE8 0000h to FFFF FFFFh	00E8 0000h to 00FF FFFFh	128 K	0000 0000h to 0001 FFFFh
1 M	FFF0 0000h to FFFF FFFFh	00F0 0000h to 00FF FFFFh	128 K	0000 0000h to 0001 FFFFh

Note: See Table 1.3, List of Products, for the product type name.

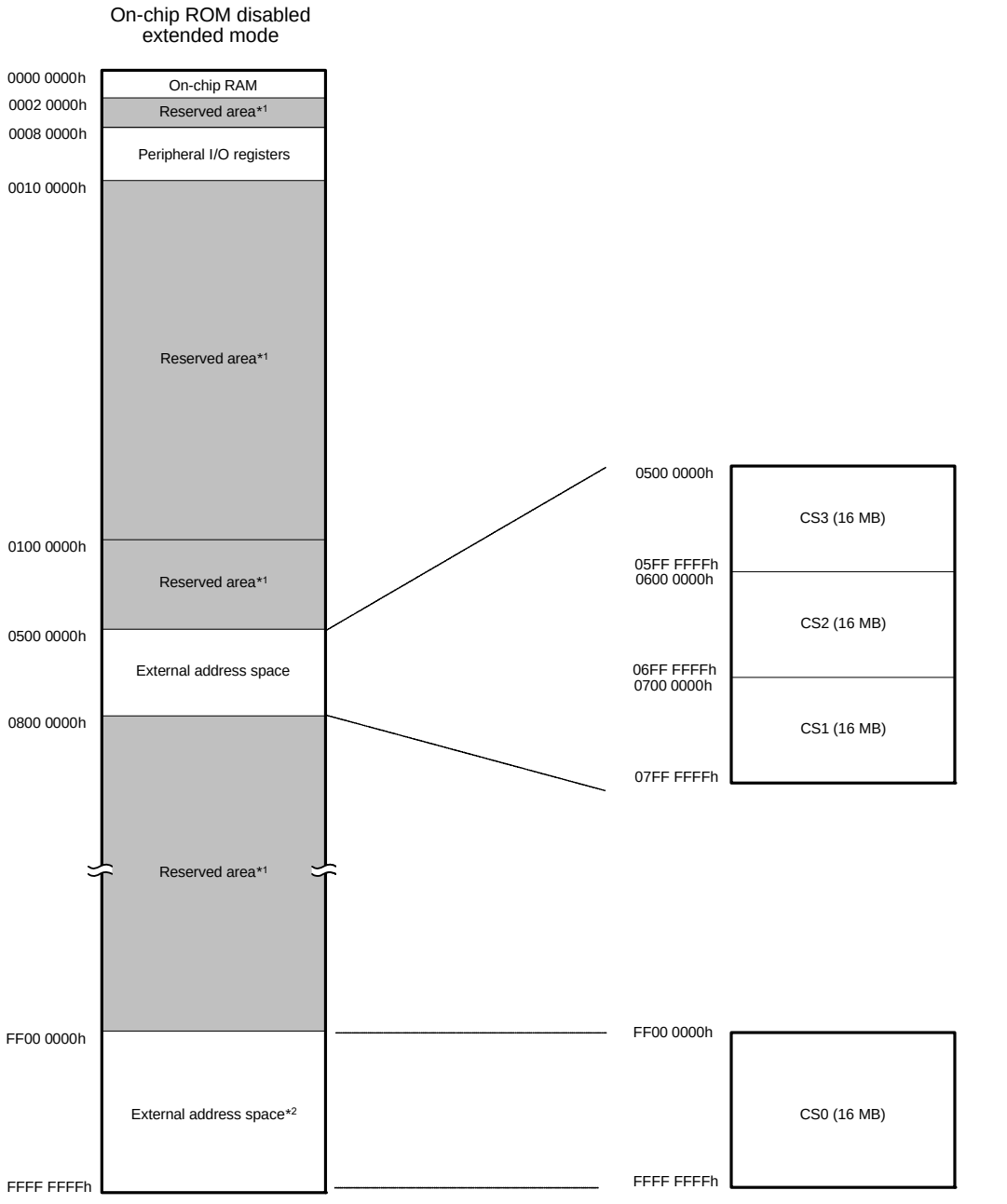
Note 3. Reserved areas should not be accessed.

Figure 3.1 Memory Map in Each Operating Mode

3.2 External Address Space

The external address space is divided into up to four CS areas (CS0 to CS3), each corresponding to the CSn# signal output from a CSn# (n = 0 to 3) pin.

Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS3) in on-chip ROM disabled extended mode.



Note 1. Reserved areas should not be accessed.

Note 2. The CS0 area is disabled in on-chip ROM enabled extended mode. In this mode, the address space for addresses above 0800 0000h is as shown in figure on this section “Memory Map in Each Operating Mode”.

Figure 3.2 Correspondence between External Address Spaces and CS Areas (In On-Chip ROM Disabled Extended Mode)

4. I/O Registers

This section gives information on the on-chip I/O register addresses. The information is given as shown below. Notes on writing to registers are also given at the end.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to module symbols.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- Among the internal I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.

(2) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.
As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERn of the ICU (interrupt request enable bit) cleared to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

(a) Write to an I/O register.
(b) Read the value from the I/O register to a general register.
(c) Execute the operation using the value read.
(d) Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.B  #SFR_DATA, [R1]
CMP    [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.W  #SFR_DATA, [R1]
CMP    [R1].W, R1
;; Next process
```

- Longword-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.L  #SFR_DATA, [R1]
CMP    [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

(3) Number of Access Cycles to I/O Registers

For the number of I/O register access cycles, refer to Table 4.1, List of I/O Registers (Address Order).
The number of access cycles to I/O registers is obtained by following equation.*1

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
Number of divided clock synchronization cycles +
Number of bus cycles for internal peripheral buses 1 to 6

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed.
When peripheral functions connected to internal peripheral bus 2 to 6 or registers for the external bus control unit (except for bus error related registers) are accessed, the number of divided clock synchronization cycles is added.
The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK, BCLK) or bus access timing.
In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access states shown in Table 4.1.
When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.
In the external bus control unit, the sum of the number of bus cycles for internal main bus 1 and the number of divided clock synchronization cycles will be one cycle of BCLK at a maximum. Therefore, one BCLK is added to the number of access cycles shown in Table 4.1.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the instruction fetching to the external memory or bus access from the different bus master (DMAC or DTC).

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 0000h	SYSTEM	Mode Monitor Register	MDMONR	16	16	3 ICLK		Operating Modes	
0008 0002h	SYSTEM	Mode Status Register	MDSR	16	16	3 ICLK			
0008 0006h	SYSTEM	System Control Register 0	SYSCR0	16	16	3 ICLK			
0008 0008h	SYSTEM	System Control Register 1	SYSCR1	16	16	3 ICLK			
0008 000Ch	SYSTEM	Standby Control Register	SBYCR	16	16	3 ICLK		Low Power Consumption	
0008 0010h	SYSTEM	Module Stop Control Register A	MSTPCRA	32	32	3 ICLK			
0008 0014h	SYSTEM	Module Stop Control Register B	MSTPCRB	32	32	3 ICLK			
0008 0018h	SYSTEM	Module Stop Control Register C	MSTPCRC	32	32	3 ICLK			
0008 0020h	SYSTEM	System Clock Control Register	SCKCR	32	32	3 ICLK		Clock Generation Circuit	
0008 0026h	SYSTEM	System Clock Control Register 3	SCKCR3	16	16	3 ICLK			
0008 0028h	SYSTEM	PLL Control Register	PLLCR	16	16	3 ICLK			
0008 002Ah	SYSTEM	PLL Control Register 2	PLLCR2	8	8	3 ICLK			
0008 0030h	SYSTEM	External Bus Clock Control Register	BCKCR	8	8	3 ICLK			
0008 0032h	SYSTEM	Main Clock Oscillator Control Register	MOSCCR	8	8	3 ICLK			
0008 0034h	SYSTEM	Low-Speed On-Chip Oscillator Control Register	LOCOCR	8	8	3 ICLK			
0008 0035h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Control Register	ILOCOCR	8	8	3 ICLK			
0008 0040h	SYSTEM	Oscillation Stop Detection Control Register	OSTDCR	8	8	3 ICLK			
0008 0041h	SYSTEM	Oscillation Stop Detection Status Register	OSTDSR	8	8	3 ICLK			
0008 00A0h	SYSTEM	Operating Power Control Register	OPCCR	8	8	3 ICLK		Low Power Consumption	
0008 00A1h	SYSTEM	Sleep Mode Return Clock Source Switching Register	RSTCKCR	8	8	3 ICLK			
0008 00A2h	SYSTEM	Main Clock Oscillator Wait Control Register	MOSCWTCR	8	8	3 ICLK			
0008 00A6h	SYSTEM	PLL Wait Control Register	PLLWTCR	8	8	3 ICLK			
0008 00C0h	SYSTEM	Reset Status Register 2	RSTSR2	8	8	3 ICLK		Resets	
0008 00C2h	SYSTEM	Software Reset Register	SWRR	16	16	3 ICLK			
0008 00E0h	SYSTEM	Voltage Monitoring 1 Circuit Control Register 1	LVD1CR1	8	8	3 ICLK		LVDA	
0008 00E1h	SYSTEM	Voltage Monitoring 1 Circuit Status Register	LVD1SR	8	8	3 ICLK			
0008 00E2h	SYSTEM	Voltage Monitoring 2 Circuit Control Register 1	LVD2CR1	8	8	3 ICLK			
0008 00E3h	SYSTEM	Voltage Monitoring 2 Circuit Status Register	LVD2SR	8	8	3 ICLK			
0008 03FEh	SYSTEM	Protect Register	PRCR	16	16	3 ICLK		Register Write Protection Function	
0008 1300h	BSC	Bus Error Status Clear Register	BERCLR	8	8	2 ICLK		Buses	
0008 1304h	BSC	Bus Error Monitoring Enable Register	BEREN	8	8	2 ICLK			
0008 1308h	BSC	Bus Error Status Register 1	BERSR1	8	8	2 ICLK			
0008 130Ah	BSC	Bus Error Status Register 2	BERSR2	16	16	2 ICLK			
0008 1310h	BSC	Bus Priority Control Register	BUSPRI	16	16	2 ICLK			
0008 2000h	DMAC0	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACA	
0008 2004h	DMAC0	DMA Destination Address Register	DMDAR	32	32	2 ICLK			
0008 2008h	DMAC0	DMA Transfer Count Register	DMCRA	32	32	2 ICLK			
0008 200Ch	DMAC0	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK			
0008 2010h	DMAC0	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK			
0008 2013h	DMAC0	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK			
0008 2014h	DMAC0	DMA Address Mode Register	DMAMD	16	16	2 ICLK			
0008 2018h	DMAC0	DMA Offset Register	DMOFR	32	32	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (2 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 201Ch	DMAC0	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACA	
0008 201Dh	DMAC0	DMA Software Start Register	DMREQ	8	8	2 ICLK			
0008 201Eh	DMAC0	DMA Status Register	DMSTS	8	8	2 ICLK			
0008 201Fh	DMAC0	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK			
0008 2040h	DMAC1	DMA Source Address Register	DMSAR	32	32	2 ICLK			
0008 2044h	DMAC1	DMA Destination Address Register	DMDAR	32	32	2 ICLK			
0008 2048h	DMAC1	DMA Transfer Count Register	DMCRA	32	32	2 ICLK			
0008 204Ch	DMAC1	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK			
0008 2050h	DMAC1	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK			
0008 2053h	DMAC1	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK			
0008 2054h	DMAC1	DMA Address Mode Register	DMAMD	16	16	2 ICLK			
0008 205Ch	DMAC1	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK			
0008 205Dh	DMAC1	DMA Software Start Register	DMREQ	8	8	2 ICLK			
0008 205Eh	DMAC1	DMA Status Register	DMSTS	8	8	2 ICLK			
0008 205Fh	DMAC1	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK			
0008 2080h	DMAC2	DMA Source Address Register	DMSAR	32	32	2 ICLK			
0008 2084h	DMAC2	DMA Destination Address Register	DMDAR	32	32	2 ICLK			
0008 2088h	DMAC2	DMA Transfer Count Register	DMCRA	32	32	2 ICLK			
0008 208Ch	DMAC2	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK			
0008 2090h	DMAC2	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK			
0008 2093h	DMAC2	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK			
0008 2094h	DMAC2	DMA Address Mode Register	DMAMD	16	16	2 ICLK			
0008 209Ch	DMAC2	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK			
0008 209Dh	DMAC2	DMA Software Start Register	DMREQ	8	8	2 ICLK			
0008 209Eh	DMAC2	DMA Status Register	DMSTS	8	8	2 ICLK			
0008 209Fh	DMAC2	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK			
0008 20C0h	DMAC3	DMA Source Address Register	DMSAR	32	32	2 ICLK			
0008 20C4h	DMAC3	DMA Destination Address Register	DMDAR	32	32	2 ICLK			
0008 20C8h	DMAC3	DMA Transfer Count Register	DMCRA	32	32	2 ICLK			
0008 20CCh	DMAC3	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK			
0008 20D0h	DMAC3	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK			
0008 20D3h	DMAC3	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK			
0008 20D4h	DMAC3	DMA Address Mode Register	DMAMD	16	16	2 ICLK			
0008 20DCh	DMAC3	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK			
0008 20DDh	DMAC3	DMA Software Start Register	DMREQ	8	8	2 ICLK			
0008 20DEh	DMAC3	DMA Status Register	DMSTS	8	8	2 ICLK			
0008 20DFh	DMAC3	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK			
0008 2200h	DMAC	DMA Module Activation Register	DMAST	8	8	2 ICLK			
0008 2400h	DTC	DTC Control Register	DTCCR	8	8	2 ICLK		DTCa	
0008 2404h	DTC	DTC Vector Base Register	DTCVBR	32	32	2 ICLK			
0008 2408h	DTC	DTC Address Mode Register	DTCADMOD	8	8	2 ICLK			
0008 240Ch	DTC	DTC Module Start Register	DTCST	8	8	2 ICLK			
0008 240Eh	DTC	DTC Status Register	DTCSTS	16	16	2 ICLK			
0008 3002h	BSC	CS0 Mode Register	CS0MOD	16	16	1 to 2BCLK		Buses	
0008 3004h	BSC	CS0 Wait Control Register 1	CS0WCR1	32	32	1 to 2BCLK			
0008 3008h	BSC	CS0 Wait Control Register 2	CS0WCR2	32	32	1 to 2BCLK			
0008 3012h	BSC	CS1 Mode Register	CS1MOD	16	16	1 to 2BCLK			
0008 3014h	BSC	CS1 Wait Control Register 1	CS1WCR1	32	32	1 to 2BCLK			
0008 3018h	BSC	CS1 Wait Control Register 2	CS1WCR2	32	32	1 to 2BCLK			

Table 4.1 List of I/O Registers (Address Order) (3 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 3022h	BSC	CS2 Mode Register	CS2MOD	16	16	1 to 2BCLK		Buses	
0008 3024h	BSC	CS2 Wait Control Register 1	CS2WCR1	32	32	1 to 2BCLK			
0008 3028h	BSC	CS2 Wait Control Register 2	CS2WCR2	32	32	1 to 2BCLK			
0008 3032h	BSC	CS3 Mode Register	CS3MOD	16	16	1 to 2BCLK			
0008 3034h	BSC	CS3 Wait Control Register 1	CS3WCR1	32	32	1 to 2BCLK			
0008 3038h	BSC	CS3 Wait Control Register 2	CS3WCR2	32	32	1 to 2BCLK			
0008 3802h	BSC	CS0 Control Register	CS0CR	16	16	1 to 2BCLK			
0008 380Ah	BSC	CS0 Recovery Cycle Register	CS0REC	16	16	1 to 2BCLK			
0008 3812h	BSC	CS1 Control Register	CS1CR	16	16	1 to 2BCLK			
0008 381Ah	BSC	CS1 Recovery Cycle Register	CS1REC	16	16	1 to 2BCLK			
0008 3822h	BSC	CS2 Control Register	CS2CR	16	16	1 to 2BCLK			
0008 382Ah	BSC	CS2 Recovery Cycle Register	CS2REC	16	16	1 to 2BCLK			
0008 3832h	BSC	CS3 Control Register	CS3CR	16	16	1 to 2BCLK			
0008 383Ah	BSC	CS3 Recovery Cycle Register	CS3REC	16	16	1 to 2BCLK			
0008 3880h	BSC	CS Recovery Cycle Insertion Enable Register	CSRECEN	16	16	1 to 2BCLK			
0008 6400h	MPU	Region-0 Start Page Number Register	RSPAGE0	32	32	1 ICLK		MPU	
0008 6404h	MPU	Region-0 End Page Number Register	REPAGE0	32	32	1 ICLK			
0008 6408h	MPU	Region-1 Start Page Number Register	RSPAGE1	32	32	1 ICLK			
0008 640Ch	MPU	Region-1 End Page Number Register	REPAGE1	32	32	1 ICLK			
0008 6410h	MPU	Region-2 Start Page Number Register	RSPAGE2	32	32	1 ICLK			
0008 6414h	MPU	Region-2 End Page Number Register	REPAGE2	32	32	1 ICLK			
0008 6418h	MPU	Region-3 Start Page Number Register	RSPAGE3	32	32	1 ICLK			
0008 641Ch	MPU	Region-3 End Page Number Register	REPAGE3	32	32	1 ICLK			
0008 6420h	MPU	Region-4 Start Page Number Register	RSPAGE4	32	32	1 ICLK			
0008 6424h	MPU	Region-4 End Page Number Register	REPAGE4	32	32	1 ICLK			
0008 6428h	MPU	Region-5 Start Page Number Register	RSPAGE5	32	32	1 ICLK			
0008 642Ch	MPU	Region-5 End Page Number Register	REPAGE5	32	32	1 ICLK			
0008 6430h	MPU	Region-6 Start Page Number Register	RSPAGE6	32	32	1 ICLK			
0008 6434h	MPU	Region-6 End Page Number Register	REPAGE6	32	32	1 ICLK			
0008 6438h	MPU	Region-7 Start Page Number Register	RSPAGE7	32	32	1 ICLK			
0008 643Ch	MPU	Region-7 End Page Number Register	REPAGE7	32	32	1 ICLK			
0008 6500h	MPU	Memory-Protection Enable Register	MPEN	32	32	1 ICLK			
0008 6504h	MPU	Background Access Control Register	MPBAC	32	32	1 ICLK			
0008 6508h	MPU	Memory-Protection Error Status-Clearing Register	MPECLR	32	32	1 ICLK			
0008 650Ch	MPU	Memory-Protection Error Status Register	MPESTS	32	32	1 ICLK			
0008 6514h	MPU	Data Memory-Protection Error Address Register	MPDEA	32	32	1 ICLK			
0008 6520h	MPU	Region Search Address Register	MPSA	32	32	1 ICLK			
0008 6524h	MPU	Region Search Operation Register	MPOPS	16	16	1 ICLK			
0008 6526h	MPU	Region Invalidation Operation Register	MPOPI	16	16	1 ICLK			
0008 6528h	MPU	Instruction-Hit Region Register	MHITI	32	32	1 ICLK			
0008 652Ch	MPU	Data-Hit Region Register	MHITD	32	32	1 ICLK			
0008 7010h	ICU	Interrupt Request Register 016	IR016	8	8	2 ICLK		ICUb	
0008 7015h	ICU	Interrupt Request Register 021	IR021	8	8	2 ICLK			
0008 7017h	ICU	Interrupt Request Register 023	IR023	8	8	2 ICLK			
0008 701Bh	ICU	Interrupt Request Register 027	IR027	8	8	2 ICLK			
0008 701Ch	ICU	Interrupt Request Register 028	IR028	8	8	2 ICLK			
0008 701Dh	ICU	Interrupt Request Register 029	IR029	8	8	2 ICLK			
0008 701Eh	ICU	Interrupt Request Register 030	IR030	8	8	2 ICLK			
0008 701Fh	ICU	Interrupt Request Register 031	IR031	8	8	2 ICLK			
0008 7020h	ICU	Interrupt Request Register 032	IR032	8	8	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (4 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 7021h	ICU	Interrupt Request Register 033	IR033	8	8	2 ICLK		ICUb	
0008 7022h	ICU	Interrupt Request Register 034	IR034	8	8	2 ICLK			
0008 702Ch	ICU	Interrupt Request Register 044	IR044	8	8	2 ICLK			
0008 702Dh	ICU	Interrupt Request Register 045	IR045	8	8	2 ICLK			
0008 702Eh	ICU	Interrupt Request Register 046	IR046	8	8	2 ICLK			
0008 702Fh	ICU	Interrupt Request Register 047	IR047	8	8	2 ICLK			
0008 7030h	ICU	Interrupt Request Register 048	IR048	8	8	2 ICLK			
0008 7031h	ICU	Interrupt Request Register 049	IR049	8	8	2 ICLK			
0008 7032h	ICU	Interrupt Request Register 050	IR050	8	8	2 ICLK			
0008 7033h	ICU	Interrupt Request Register 051	IR051	8	8	2 ICLK			
0008 7039h	ICU	Interrupt Request Register 057	IR057	8	8	2 ICLK			
0008 7040h	ICU	Interrupt Request Register 064	IR064	8	8	2 ICLK			
0008 7041h	ICU	Interrupt Request Register 065	IR065	8	8	2 ICLK			
0008 7042h	ICU	Interrupt Request Register 066	IR066	8	8	2 ICLK			
0008 7043h	ICU	Interrupt Request Register 067	IR067	8	8	2 ICLK			
0008 7044h	ICU	Interrupt Request Register 068	IR068	8	8	2 ICLK			
0008 7045h	ICU	Interrupt Request Register 069	IR069	8	8	2 ICLK			
0008 7046h	ICU	Interrupt Request Register 070	IR070	8	8	2 ICLK			
0008 7047h	ICU	Interrupt Request Register 071	IR071	8	8	2 ICLK			
0008 7048h	ICU	Interrupt Request Register 072	IR072	8	8	2 ICLK			
0008 7049h	ICU	Interrupt Request Register 073	IR073	8	8	2 ICLK			
0008 704Ah	ICU	Interrupt Request Register 074	IR074	8	8	2 ICLK			
0008 704Bh	ICU	Interrupt Request Register 075	IR075	8	8	2 ICLK			
0008 704Ch	ICU	Interrupt Request Register 076	IR076	8	8	2 ICLK			
0008 704Dh	ICU	Interrupt Request Register 077	IR077	8	8	2 ICLK			Not available in 5-V packages.
0008 704Eh	ICU	Interrupt Request Register 078	IR078	8	8	2 ICLK			Not available in 5-V packages.
0008 704Fh	ICU	Interrupt Request Register 079	IR079	8	8	2 ICLK			Not available in 5-V packages.
0008 705Eh	ICU	Interrupt Request Register 094	IR094	8	8	2 ICLK			Not available in 5-V packages.
0008 705Fh	ICU	Interrupt Request Register 095	IR095	8	8	2 ICLK			Not available in 5-V packages.
0008 7062h	ICU	Interrupt Request Register 098	IR098	8	8	2 ICLK			
0008 7063h	ICU	Interrupt Request Register 099	IR099	8	8	2 ICLK			
0008 7064h	ICU	Interrupt Request Register 100	IR100	8	8	2 ICLK			
0008 7065h	ICU	Interrupt Request Register 101	IR101	8	8	2 ICLK			
0008 7066h	ICU	Interrupt Request Register 102	IR102	8	8	2 ICLK			
0008 7067h	ICU	Interrupt Request Register 103	IR103	8	8	2 ICLK			
0008 706Ah	ICU	Interrupt Request Register 106	IR106	8	8	2 ICLK			
0008 706Bh	ICU	Interrupt Request Register 107	IR107	8	8	2 ICLK			
0008 706Fh	ICU	Interrupt Request Register 111	IR111	8	8	2 ICLK			Not available in 5-V packages.
0008 7070h	ICU	Interrupt Request Register 112	IR112	8	8	2 ICLK			Not available in 5-V packages.
0008 7071h	ICU	Interrupt Request Register 113	IR113	8	8	2 ICLK			Not available in 5-V packages.
0008 7072h	ICU	Interrupt Request Register 114	IR114	8	8	2 ICLK			
0008 7073h	ICU	Interrupt Request Register 115	IR115	8	8	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (5 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 7074h	ICU	Interrupt Request Register 116	IR116	8	8	2 ICLK		ICUb	
0008 7075h	ICU	Interrupt Request Register 117	IR117	8	8	2 ICLK			
0008 7076h	ICU	Interrupt Request Register 118	IR118	8	8	2 ICLK			
0008 7077h	ICU	Interrupt Request Register 119	IR119	8	8	2 ICLK			
0008 7078h	ICU	Interrupt Request Register 120	IR120	8	8	2 ICLK			
0008 7079h	ICU	Interrupt Request Register 121	IR121	8	8	2 ICLK			
0008 707Ah	ICU	Interrupt Request Register 122	IR122	8	8	2 ICLK			
0008 707Bh	ICU	Interrupt Request Register 123	IR123	8	8	2 ICLK			
0008 707Ch	ICU	Interrupt Request Register 124	IR124	8	8	2 ICLK			
0008 707Dh	ICU	Interrupt Request Register 125	IR125	8	8	2 ICLK			
0008 707Eh	ICU	Interrupt Request Register 126	IR126	8	8	2 ICLK			
0008 707Fh	ICU	Interrupt Request Register 127	IR127	8	8	2 ICLK			
0008 7080h	ICU	Interrupt Request Register 128	IR128	8	8	2 ICLK			
0008 7081h	ICU	Interrupt Request Register 129	IR129	8	8	2 ICLK			
0008 7082h	ICU	Interrupt Request Register 130	IR130	8	8	2 ICLK			
0008 7083h	ICU	Interrupt Request Register 131	IR131	8	8	2 ICLK			
0008 7084h	ICU	Interrupt Request Register 132	IR132	8	8	2 ICLK			
0008 7085h	ICU	Interrupt Request Register 133	IR133	8	8	2 ICLK			
0008 7086h	ICU	Interrupt Request Register 134	IR134	8	8	2 ICLK			
0008 7087h	ICU	Interrupt Request Register 135	IR135	8	8	2 ICLK			
0008 7088h	ICU	Interrupt Request Register 136	IR136	8	8	2 ICLK			
0008 7089h	ICU	Interrupt Request Register 137	IR137	8	8	2 ICLK			
0008 708Ah	ICU	Interrupt Request Register 138	IR138	8	8	2 ICLK			
0008 708Bh	ICU	Interrupt Request Register 139	IR139	8	8	2 ICLK			
0008 708Ch	ICU	Interrupt Request Register 140	IR140	8	8	2 ICLK			
0008 708Dh	ICU	Interrupt Request Register 141	IR141	8	8	2 ICLK			
0008 708Eh	ICU	Interrupt Request Register 142	IR142	8	8	2 ICLK			
0008 708Fh	ICU	Interrupt Request Register 143	IR143	8	8	2 ICLK			
0008 7090h	ICU	Interrupt Request Register 144	IR144	8	8	2 ICLK			
0008 7091h	ICU	Interrupt Request Register 145	IR145	8	8	2 ICLK			
0008 7092h	ICU	Interrupt Request Register 146	IR146	8	8	2 ICLK			
0008 7093h	ICU	Interrupt Request Register 147	IR147	8	8	2 ICLK			
0008 7094h	ICU	Interrupt Request Register 148	IR148	8	8	2 ICLK			
0008 7095h	ICU	Interrupt Request Register 149	IR149	8	8	2 ICLK			
0008 7096h	ICU	Interrupt Request Register 150	IR150	8	8	2 ICLK			
0008 7097h	ICU	Interrupt Request Register 151	IR151	8	8	2 ICLK			
0008 7098h	ICU	Interrupt Request Register 152	IR152	8	8	2 ICLK			
0008 7099h	ICU	Interrupt Request Register 153	IR153	8	8	2 ICLK			
0008 709Ah	ICU	Interrupt Request Register 154	IR154	8	8	2 ICLK			
0008 709Bh	ICU	Interrupt Request Register 155	IR155	8	8	2 ICLK			
0008 709Ch	ICU	Interrupt Request Register 156	IR156	8	8	2 ICLK			
0008 709Dh	ICU	Interrupt Request Register 157	IR157	8	8	2 ICLK			
0008 709Eh	ICU	Interrupt Request Register 158	IR158	8	8	2 ICLK			
0008 709Fh	ICU	Interrupt Request Register 159	IR159	8	8	2 ICLK			
0008 70A0h	ICU	Interrupt Request Register 160	IR160	8	8	2 ICLK			
0008 70A1h	ICU	Interrupt Request Register 161	IR161	8	8	2 ICLK			
0008 70A2h	ICU	Interrupt Request Register 162	IR162	8	8	2 ICLK			
0008 70A3h	ICU	Interrupt Request Register 163	IR163	8	8	2 ICLK			
0008 70A4h	ICU	Interrupt Request Register 164	IR164	8	8	2 ICLK			
0008 70A5h	ICU	Interrupt Request Register 165	IR165	8	8	2 ICLK			
0008 70A6h	ICU	Interrupt Request Register 166	IR166	8	8	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (6 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 70A7h	ICU	Interrupt Request Register 167	IR167	8	8	2 ICLK		ICUb	
0008 70AAh	ICU	Interrupt Request Register 170	IR170	8	8	2 ICLK			
0008 70ABh	ICU	Interrupt Request Register 171	IR171	8	8	2 ICLK			
0008 70AEh	ICU	Interrupt Request Register 174	IR174	8	8	2 ICLK			
0008 70AFh	ICU	Interrupt Request Register 175	IR175	8	8	2 ICLK			
0008 70B0h	ICU	Interrupt Request Register 176	IR176	8	8	2 ICLK			
0008 70B1h	ICU	Interrupt Request Register 177	IR177	8	8	2 ICLK			
0008 70B2h	ICU	Interrupt Request Register 178	IR178	8	8	2 ICLK			
0008 70B3h	ICU	Interrupt Request Register 179	IR179	8	8	2 ICLK			
0008 70B4h	ICU	Interrupt Request Register 180	IR180	8	8	2 ICLK			
0008 70B5h	ICU	Interrupt Request Register 181	IR181	8	8	2 ICLK			
0008 70B6h	ICU	Interrupt Request Register 182	IR182	8	8	2 ICLK			
0008 70B7h	ICU	Interrupt Request Register 183	IR183	8	8	2 ICLK			
0008 70B8h	ICU	Interrupt Request Register 184	IR184	8	8	2 ICLK			
0008 70B9h	ICU	Interrupt Request Register 185	IR185	8	8	2 ICLK			
0008 70BAh	ICU	Interrupt Request Register 186	IR186	8	8	2 ICLK			
0008 70BBh	ICU	Interrupt Request Register 187	IR187	8	8	2 ICLK			
0008 70BCh	ICU	Interrupt Request Register 188	IR188	8	8	2 ICLK			
0008 70BDh	ICU	Interrupt Request Register 189	IR189	8	8	2 ICLK			
0008 70BEh	ICU	Interrupt Request Register 190	IR190	8	8	2 ICLK			
0008 70BFh	ICU	Interrupt Request Register 191	IR191	8	8	2 ICLK			
0008 70C0h	ICU	Interrupt Request Register 192	IR192	8	8	2 ICLK			
0008 70C1h	ICU	Interrupt Request Register 193	IR193	8	8	2 ICLK			
0008 70C2h	ICU	Interrupt Request Register 194	IR194	8	8	2 ICLK			
0008 70C3h	ICU	Interrupt Request Register 195	IR195	8	8	2 ICLK			
0008 70C4h	ICU	Interrupt Request Register 196	IR196	8	8	2 ICLK			
0008 70C5h	ICU	Interrupt Request Register 197	IR197	8	8	2 ICLK			
0008 70C6h	ICU	Interrupt Request Register 198	IR198	8	8	2 ICLK			
0008 70C7h	ICU	Interrupt Request Register 199	IR199	8	8	2 ICLK			
0008 70C8h	ICU	Interrupt Request Register 200	IR200	8	8	2 ICLK			
0008 70C9h	ICU	Interrupt Request Register 201	IR201	8	8	2 ICLK			
0008 70CAh	ICU	Interrupt Request Register 202	IR202	8	8	2 ICLK			
0008 70CBh	ICU	Interrupt Request Register 203	IR203	8	8	2 ICLK			
0008 70CCh	ICU	Interrupt Request Register 204	IR204	8	8	2 ICLK			
0008 70CDh	ICU	Interrupt Request Register 205	IR205	8	8	2 ICLK			
0008 70CEh	ICU	Interrupt Request Register 206	IR206	8	8	2 ICLK			
0008 70CFh	ICU	Interrupt Request Register 207	IR207	8	8	2 ICLK			
0008 70D0h	ICU	Interrupt Request Register 208	IR208	8	8	2 ICLK			
0008 70D1h	ICU	Interrupt Request Register 209	IR209	8	8	2 ICLK			
0008 70D2h	ICU	Interrupt Request Register 210	IR210	8	8	2 ICLK			
0008 70D3h	ICU	Interrupt Request Register 211	IR211	8	8	2 ICLK			
0008 70D4h	ICU	Interrupt Request Register 212	IR212	8	8	2 ICLK			
0008 70D5h	ICU	Interrupt Request Register 213	IR213	8	8	2 ICLK			
0008 70D6h	ICU	Interrupt Request Register 214	IR214	8	8	2 ICLK			
0008 70D7h	ICU	Interrupt Request Register 215	IR215	8	8	2 ICLK			
0008 70D8h	ICU	Interrupt Request Register 216	IR216	8	8	2 ICLK			
0008 70D9h	ICU	Interrupt Request Register 217	IR217	8	8	2 ICLK			
0008 70DAh	ICU	Interrupt Request Register 218	IR218	8	8	2 ICLK			
0008 70DBh	ICU	Interrupt Request Register 219	IR219	8	8	2 ICLK			
0008 70DCh	ICU	Interrupt Request Register 220	IR220	8	8	2 ICLK			
0008 70DDh	ICU	Interrupt Request Register 221	IR221	8	8	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (7 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 70DEh	ICU	Interrupt Request Register 222	IR222	8	8	2 ICLK		ICUb	
0008 70DFh	ICU	Interrupt Request Register 223	IR223	8	8	2 ICLK			
0008 70E0h	ICU	Interrupt Request Register 224	IR224	8	8	2 ICLK			
0008 70E1h	ICU	Interrupt Request Register 225	IR225	8	8	2 ICLK			
0008 70E2h	ICU	Interrupt Request Register 226	IR226	8	8	2 ICLK			
0008 70E3h	ICU	Interrupt Request Register 227	IR227	8	8	2 ICLK			
0008 70E4h	ICU	Interrupt Request Register 228	IR228	8	8	2 ICLK			
0008 70E5h	ICU	Interrupt Request Register 229	IR229	8	8	2 ICLK			
0008 70E6h	ICU	Interrupt Request Register 230	IR230	8	8	2 ICLK			
0008 70E7h	ICU	Interrupt Request Register 231	IR231	8	8	2 ICLK			
0008 70E8h	ICU	Interrupt Request Register 232	IR232	8	8	2 ICLK			
0008 70E9h	ICU	Interrupt Request Register 233	IR233	8	8	2 ICLK			
0008 70EAh	ICU	Interrupt Request Register 234	IR234	8	8	2 ICLK			
0008 70EBh	ICU	Interrupt Request Register 235	IR235	8	8	2 ICLK			
0008 70ECh	ICU	Interrupt Request Register 236	IR236	8	8	2 ICLK			
0008 70EDh	ICU	Interrupt Request Register 237	IR237	8	8	2 ICLK			
0008 70EEh	ICU	Interrupt Request Register 238	IR238	8	8	2 ICLK			
0008 70EFh	ICU	Interrupt Request Register 239	IR239	8	8	2 ICLK			
0008 70F0h	ICU	Interrupt Request Register 240	IR240	8	8	2 ICLK			
0008 70F1h	ICU	Interrupt Request Register 241	IR241	8	8	2 ICLK			
0008 70F2h	ICU	Interrupt Request Register 242	IR242	8	8	2 ICLK			
0008 70F3h	ICU	Interrupt Request Register 243	IR243	8	8	2 ICLK			
0008 70F4h	ICU	Interrupt Request Register 244	IR244	8	8	2 ICLK			
0008 70F5h	ICU	Interrupt Request Register 245	IR245	8	8	2 ICLK			
0008 70F6h	ICU	Interrupt Request Register 246	IR246	8	8	2 ICLK			
0008 70F7h	ICU	Interrupt Request Register 247	IR247	8	8	2 ICLK			
0008 70F8h	ICU	Interrupt Request Register 248	IR248	8	8	2 ICLK			
0008 70F9h	ICU	Interrupt Request Register 249	IR249	8	8	2 ICLK			
0008 70FAh	ICU	Interrupt Request Register 250	IR250	8	8	2 ICLK			
0008 70FBh	ICU	Interrupt Request Register 251	IR251	8	8	2 ICLK			
0008 70FCh	ICU	Interrupt Request Register 252	IR252	8	8	2 ICLK			
0008 70FDh	ICU	Interrupt Request Register 253	IR253	8	8	2 ICLK			
0008 711Bh	ICU	DTC Activation Enable Register 027	DTCER027	8	8	2 ICLK			
0008 711Ch	ICU	DTC Activation Enable Register 028	DTCER028	8	8	2 ICLK			
0008 711Dh	ICU	DTC Activation Enable Register 029	DTCER029	8	8	2 ICLK			
0008 711Eh	ICU	DTC Activation Enable Register 030	DTCER030	8	8	2 ICLK			
0008 711Fh	ICU	DTC Activation Enable Register 031	DTCER031	8	8	2 ICLK			
0008 712Dh	ICU	DTC Activation Enable Register 045	DTCER045	8	8	2 ICLK			
0008 712Eh	ICU	DTC Activation Enable Register 046	DTCER046	8	8	2 ICLK			
0008 7131h	ICU	DTC Activation Enable Register 049	DTCER049	8	8	2 ICLK			
0008 7132h	ICU	DTC Activation Enable Register 050	DTCER050	8	8	2 ICLK			
0008 7140h	ICU	DTC Activation Enable Register 064	DTCER064	8	8	2 ICLK			
0008 7141h	ICU	DTC Activation Enable Register 065	DTCER065	8	8	2 ICLK			
0008 7142h	ICU	DTC Activation Enable Register 066	DTCER066	8	8	2 ICLK			
0008 7143h	ICU	DTC Activation Enable Register 067	DTCER067	8	8	2 ICLK			
0008 7144h	ICU	DTC Activation Enable Register 068	DTCER068	8	8	2 ICLK			
0008 7145h	ICU	DTC Activation Enable Register 069	DTCER069	8	8	2 ICLK			
0008 7146h	ICU	DTC Activation Enable Register 070	DTCER070	8	8	2 ICLK			
0008 7147h	ICU	DTC Activation Enable Register 071	DTCER071	8	8	2 ICLK			
0008 7148h	ICU	DTC Activation Enable Register 072	DTCER072	8	8	2 ICLK			
0008 7149h	ICU	DTC Activation Enable Register 073	DTCER073	8	8	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (8 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 714Ah	ICU	DTC Activation Enable Register 074	DTCER074	8	8	2 ICLK		ICUb	
0008 714Bh	ICU	DTC Activation Enable Register 075	DTCER075	8	8	2 ICLK			
0008 714Ch	ICU	DTC Activation Enable Register 076	DTCER076	8	8	2 ICLK			
0008 714Dh	ICU	DTC Activation Enable Register 077	DTCER077	8	8	2 ICLK			Not available in 5-V packages.
0008 714Eh	ICU	DTC Activation Enable Register 078	DTCER078	8	8	2 ICLK			Not available in 5-V packages.
0008 714Fh	ICU	DTC Activation Enable Register 079	DTCER079	8	8	2 ICLK			Not available in 5-V packages.
0008 7163h	ICU	DTC Activation Enable Register 099	DTCER099	8	8	2 ICLK			
0008 7164h	ICU	DTC Activation Enable Register 100	DTCER100	8	8	2 ICLK			
0008 7166h	ICU	DTC Activation Enable Register 102	DTCER102	8	8	2 ICLK			
0008 7167h	ICU	DTC Activation Enable Register 103	DTCER103	8	8	2 ICLK			
0008 716Ah	ICU	DTC Activation Enable Register 106	DTCER106	8	8	2 ICLK			
0008 716Bh	ICU	DTC Activation Enable Register 107	DTCER107	8	8	2 ICLK			
0008 716Fh	ICU	DTC Activation Enable Register 111	DTCER111	8	8	2 ICLK			Not available in 5-V packages.
0008 7170h	ICU	DTC Activation Enable Register 112	DTCER112	8	8	2 ICLK			Not available in 5-V packages.
0008 7172h	ICU	DTC Activation Enable Register 114	DTCER114	8	8	2 ICLK			
0008 7173h	ICU	DTC Activation Enable Register 115	DTCER115	8	8	2 ICLK			
0008 7174h	ICU	DTC Activation Enable Register 116	DTCER116	8	8	2 ICLK			
0008 7175h	ICU	DTC Activation Enable Register 117	DTCER117	8	8	2 ICLK			
0008 7179h	ICU	DTC Activation Enable Register 121	DTCER121	8	8	2 ICLK			
0008 717Ah	ICU	DTC Activation Enable Register 122	DTCER122	8	8	2 ICLK			
0008 717Dh	ICU	DTC Activation Enable Register 125	DTCER125	8	8	2 ICLK			
0008 717Eh	ICU	DTC Activation Enable Register 126	DTCER126	8	8	2 ICLK			
0008 7181h	ICU	DTC Activation Enable Register 129	DTCER129	8	8	2 ICLK			
0008 7182h	ICU	DTC Activation Enable Register 130	DTCER130	8	8	2 ICLK			
0008 7183h	ICU	DTC Activation Enable Register 131	DTCER131	8	8	2 ICLK			
0008 7184h	ICU	DTC Activation Enable Register 132	DTCER132	8	8	2 ICLK			
0008 7186h	ICU	DTC Activation Enable Register 134	DTCER134	8	8	2 ICLK			
0008 7187h	ICU	DTC Activation Enable Register 135	DTCER135	8	8	2 ICLK			
0008 7188h	ICU	DTC Activation Enable Register 136	DTCER136	8	8	2 ICLK			
0008 7189h	ICU	DTC Activation Enable Register 137	DTCER137	8	8	2 ICLK			
0008 718Ah	ICU	DTC Activation Enable Register 138	DTCER138	8	8	2 ICLK			
0008 718Bh	ICU	DTC Activation Enable Register 139	DTCER139	8	8	2 ICLK			
0008 718Ch	ICU	DTC Activation Enable Register 140	DTCER140	8	8	2 ICLK			
0008 718Dh	ICU	DTC Activation Enable Register 141	DTCER141	8	8	2 ICLK			
0008 718Eh	ICU	DTC Activation Enable Register 142	DTCER142	8	8	2 ICLK			
0008 718Fh	ICU	DTC Activation Enable Register 143	DTCER143	8	8	2 ICLK			
0008 7190h	ICU	DTC Activation Enable Register 144	DTCER144	8	8	2 ICLK			
0008 7191h	ICU	DTC Activation Enable Register 145	DTCER145	8	8	2 ICLK			
0008 7193h	ICU	DTC Activation Enable Register 147	DTCER147	8	8	2 ICLK			
0008 7194h	ICU	DTC Activation Enable Register 148	DTCER148	8	8	2 ICLK			
0008 7197h	ICU	DTC Activation Enable Register 151	DTCER151	8	8	2 ICLK			
0008 7198h	ICU	DTC Activation Enable Register 152	DTCER152	8	8	2 ICLK			
0008 719Bh	ICU	DTC Activation Enable Register 155	DTCER155	8	8	2 ICLK			
0008 719Ch	ICU	DTC Activation Enable Register 156	DTCER156	8	8	2 ICLK			
0008 719Dh	ICU	DTC Activation Enable Register 157	DTCER157	8	8	2 ICLK			
0008 719Eh	ICU	DTC Activation Enable Register 158	DTCER158	8	8	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (9 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 71A0h	ICU	DTC Activation Enable Register 160	DTCER160	8	8	2 ICLK		ICUb	
0008 71A1h	ICU	DTC Activation Enable Register 161	DTCER161	8	8	2 ICLK			
0008 71A4h	ICU	DTC Activation Enable Register 164	DTCER164	8	8	2 ICLK			
0008 71A5h	ICU	DTC Activation Enable Register 165	DTCER165	8	8	2 ICLK			
0008 71AEh	ICU	DTC Activation Enable Register 174	DTCER174	8	8	2 ICLK			
0008 71AFh	ICU	DTC Activation Enable Register 175	DTCER175	8	8	2 ICLK			
0008 71B1h	ICU	DTC Activation Enable Register 177	DTCER177	8	8	2 ICLK			
0008 71B2h	ICU	DTC Activation Enable Register 178	DTCER178	8	8	2 ICLK			
0008 71B4h	ICU	DTC Activation Enable Register 180	DTCER180	8	8	2 ICLK			
0008 71B5h	ICU	DTC Activation Enable Register 181	DTCER181	8	8	2 ICLK			
0008 71B7h	ICU	DTC Activation Enable Register 183	DTCER183	8	8	2 ICLK			
0008 71B8h	ICU	DTC Activation Enable Register 184	DTCER184	8	8	2 ICLK			
0008 71BBh	ICU	DTC Activation Enable Register 187	DTCER187	8	8	2 ICLK			
0008 71BCh	ICU	DTC Activation Enable Register 188	DTCER188	8	8	2 ICLK			
0008 71BFh	ICU	DTC Activation Enable Register 191	DTCER191	8	8	2 ICLK			
0008 71C0h	ICU	DTC Activation Enable Register 192	DTCER192	8	8	2 ICLK			
0008 71C3h	ICU	DTC Activation Enable Register 195	DTCER195	8	8	2 ICLK			
0008 71C4h	ICU	DTC Activation Enable Register 196	DTCER196	8	8	2 ICLK			
0008 71C6h	ICU	DTC Activation Enable Register 198	DTCER198	8	8	2 ICLK			
0008 71C7h	ICU	DTC Activation Enable Register 199	DTCER199	8	8	2 ICLK			
0008 71C8h	ICU	DTC Activation Enable Register 200	DTCER200	8	8	2 ICLK			
0008 71C9h	ICU	DTC Activation Enable Register 201	DTCER201	8	8	2 ICLK			
0008 71CBh	ICU	DTC Activation Enable Register 203	DTCER203	8	8	2 ICLK			
0008 71CCh	ICU	DTC Activation Enable Register 204	DTCER204	8	8	2 ICLK			
0008 71CFh	ICU	DTC Activation Enable Register 207	DTCER207	8	8	2 ICLK			
0008 71D0h	ICU	DTC Activation Enable Register 208	DTCER208	8	8	2 ICLK			
0008 71D3h	ICU	DTC Activation Enable Register 211	DTCER211	8	8	2 ICLK			
0008 71D4h	ICU	DTC Activation Enable Register 212	DTCER212	8	8	2 ICLK			
0008 71D7h	ICU	DTC Activation Enable Register 215	DTCER215	8	8	2 ICLK			
0008 71D8h	ICU	DTC Activation Enable Register 216	DTCER216	8	8	2 ICLK			
0008 71DBh	ICU	DTC Activation Enable Register 219	DTCER219	8	8	2 ICLK			
0008 71DCh	ICU	DTC Activation Enable Register 220	DTCER220	8	8	2 ICLK			
0008 71DFh	ICU	DTC Activation Enable Register 223	DTCER223	8	8	2 ICLK			
0008 71E0h	ICU	DTC Activation Enable Register 224	DTCER224	8	8	2 ICLK			
0008 71E3h	ICU	DTC Activation Enable Register 227	DTCER227	8	8	2 ICLK			
0008 71E4h	ICU	DTC Activation Enable Register 228	DTCER228	8	8	2 ICLK			
0008 71E7h	ICU	DTC Activation Enable Register 231	DTCER231	8	8	2 ICLK			
0008 71E8h	ICU	DTC Activation Enable Register 232	DTCER232	8	8	2 ICLK			
0008 71EBh	ICU	DTC Activation Enable Register 235	DTCER235	8	8	2 ICLK			
0008 71ECh	ICU	DTC Activation Enable Register 236	DTCER236	8	8	2 ICLK			
0008 71EFh	ICU	DTC Activation Enable Register 239	DTCER239	8	8	2 ICLK			
0008 71F0h	ICU	DTC Activation Enable Register 240	DTCER240	8	8	2 ICLK			
0008 71F7h	ICU	DTC Activation Enable Register 247	DTCER247	8	8	2 ICLK			
0008 71F8h	ICU	DTC Activation Enable Register 248	DTCER248	8	8	2 ICLK			
0008 71FBh	ICU	DTC Activation Enable Register 251	DTCER251	8	8	2 ICLK			
0008 71FCh	ICU	DTC Activation Enable Register 252	DTCER252	8	8	2 ICLK			
0008 7202h	ICU	Interrupt Request Enable Register 02	IER02	8	8	2 ICLK			
0008 7203h	ICU	Interrupt Request Enable Register 03	IER03	8	8	2 ICLK			
0008 7204h	ICU	Interrupt Request Enable Register 04	IER04	8	8	2 ICLK			
0008 7205h	ICU	Interrupt Request Enable Register 05	IER05	8	8	2 ICLK			
0008 7206h	ICU	Interrupt Request Enable Register 06	IER06	8	8	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (10 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 7207h	ICU	Interrupt Request Enable Register 07	IER07	8	8	2 ICLK		ICUb	
0008 7208h	ICU	Interrupt Request Enable Register 08	IER08	8	8	2 ICLK			
0008 7209h	ICU	Interrupt Request Enable Register 09	IER09	8	8	2 ICLK			
0008 720Bh	ICU	Interrupt Request Enable Register 0B	IER0B	8	8	2 ICLK			
0008 720Ch	ICU	Interrupt Request Enable Register 0C	IER0C	8	8	2 ICLK			
0008 720Dh	ICU	Interrupt Request Enable Register 0D	IER0D	8	8	2 ICLK			
0008 720Eh	ICU	Interrupt Request Enable Register 0E	IER0E	8	8	2 ICLK			
0008 720Fh	ICU	Interrupt Request Enable Register 0F	IER0F	8	8	2 ICLK			
0008 7210h	ICU	Interrupt Request Enable Register 10	IER10	8	8	2 ICLK			
0008 7211h	ICU	Interrupt Request Enable Register 11	IER11	8	8	2 ICLK			
0008 7212h	ICU	Interrupt Request Enable Register 12	IER12	8	8	2 ICLK			
0008 7213h	ICU	Interrupt Request Enable Register 13	IER13	8	8	2 ICLK			
0008 7214h	ICU	Interrupt Request Enable Register 14	IER14	8	8	2 ICLK			
0008 7215h	ICU	Interrupt Request Enable Register 15	IER15	8	8	2 ICLK			
0008 7216h	ICU	Interrupt Request Enable Register 16	IER16	8	8	2 ICLK			
0008 7217h	ICU	Interrupt Request Enable Register 17	IER17	8	8	2 ICLK			
0008 7218h	ICU	Interrupt Request Enable Register 18	IER18	8	8	2 ICLK			
0008 7219h	ICU	Interrupt Request Enable Register 19	IER19	8	8	2 ICLK			
0008 721Ah	ICU	Interrupt Request Enable Register 1A	IER1A	8	8	2 ICLK			
0008 721Bh	ICU	Interrupt Request Enable Register 1B	IER1B	8	8	2 ICLK			
0008 721Ch	ICU	Interrupt Request Enable Register 1C	IER1C	8	8	2 ICLK			
0008 721Dh	ICU	Interrupt Request Enable Register 1D	IER1D	8	8	2 ICLK			
0008 721Eh	ICU	Interrupt Request Enable Register 1E	IER1E	8	8	2 ICLK			
0008 721Fh	ICU	Interrupt Request Enable Register 1F	IER1F	8	8	2 ICLK			
0008 72E0h	ICU	Software Interrupt Activation Register	SWINTR	8	8	2 ICLK			
0008 72F0h	ICU	Fast Interrupt Set Register	FIR	16	16	2 ICLK			
0008 7300h	ICU	Interrupt Source Priority Register 000	IPR000	8	8	2 ICLK			
0008 7301h	ICU	Interrupt Source Priority Register 001	IPR001	8	8	2 ICLK			
0008 7302h	ICU	Interrupt Source Priority Register 002	IPR002	8	8	2 ICLK			
0008 7303h	ICU	Interrupt Source Priority Register 003	IPR003	8	8	2 ICLK			
0008 7304h	ICU	Interrupt Source Priority Register 004	IPR004	8	8	2 ICLK			
0008 7305h	ICU	Interrupt Source Priority Register 005	IPR005	8	8	2 ICLK			
0008 7306h	ICU	Interrupt Source Priority Register 006	IPR006	8	8	2 ICLK			
0008 7307h	ICU	Interrupt Source Priority Register 007	IPR007	8	8	2 ICLK			
0008 7320h	ICU	Interrupt Source Priority Register 032	IPR032	8	8	2 ICLK			
0008 7321h	ICU	Interrupt Source Priority Register 033	IPR033	8	8	2 ICLK			
0008 7322h	ICU	Interrupt Source Priority Register 034	IPR034	8	8	2 ICLK			
0008 732Ch	ICU	Interrupt Source Priority Register 044	IPR044	8	8	2 ICLK			
0008 7330h	ICU	Interrupt Source Priority Register 048	IPR048	8	8	2 ICLK			
0008 7339h	ICU	Interrupt Source Priority Register 057	IPR057	8	8	2 ICLK			
0008 7340h	ICU	Interrupt Source Priority Register 064	IPR064	8	8	2 ICLK			
0008 7341h	ICU	Interrupt Source Priority Register 065	IPR065	8	8	2 ICLK			
0008 7342h	ICU	Interrupt Source Priority Register 066	IPR066	8	8	2 ICLK			
0008 7343h	ICU	Interrupt Source Priority Register 067	IPR067	8	8	2 ICLK			
0008 7344h	ICU	Interrupt Source Priority Register 068	IPR068	8	8	2 ICLK			
0008 7345h	ICU	Interrupt Source Priority Register 069	IPR069	8	8	2 ICLK			
0008 7346h	ICU	Interrupt Source Priority Register 070	IPR070	8	8	2 ICLK			
0008 7347h	ICU	Interrupt Source Priority Register 071	IPR071	8	8	2 ICLK			
0008 7348h	ICU	Interrupt Source Priority Register 072	IPR072	8	8	2 ICLK			
0008 7349h	ICU	Interrupt Source Priority Register 073	IPR073	8	8	2 ICLK			
0008 734Ah	ICU	Interrupt Source Priority Register 074	IPR074	8	8	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (11 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 734Bh	ICU	Interrupt Source Priority Register 075	IPR075	8	8	2 ICLK		ICUb	
0008 734Ch	ICU	Interrupt Source Priority Register 076	IPR076	8	8	2 ICLK			
0008 734Dh	ICU	Interrupt Source Priority Register 077	IPR077	8	8	2 ICLK			Not available in 5-V packages.
0008 734Eh	ICU	Interrupt Source Priority Register 078	IPR078	8	8	2 ICLK			Not available in 5-V packages.
0008 734Fh	ICU	Interrupt Source Priority Register 079	IPR079	8	8	2 ICLK			Not available in 5-V packages.
0008 735Eh	ICU	Interrupt Source Priority Register 094	IPR094	8	8	2 ICLK			Not available in 5-V packages.
0008 735Fh	ICU	Interrupt Source Priority Register 095	IPR095	8	8	2 ICLK			Not available in 5-V packages.
0008 7362h	ICU	Interrupt Source Priority Register 098	IPR098	8	8	2 ICLK			
0008 7363h	ICU	Interrupt Source Priority Register 099	IPR099	8	8	2 ICLK			
0008 7364h	ICU	Interrupt Source Priority Register 100	IPR100	8	8	2 ICLK			
0008 7365h	ICU	Interrupt Source Priority Register 101	IPR101	8	8	2 ICLK			
0008 7366h	ICU	Interrupt Source Priority Register 102	IPR102	8	8	2 ICLK			
0008 7367h	ICU	Interrupt Source Priority Register 103	IPR103	8	8	2 ICLK			
0008 736Ah	ICU	Interrupt Source Priority Register 106	IPR106	8	8	2 ICLK			
0008 736Bh	ICU	Interrupt Source Priority Register 107	IPR107	8	8	2 ICLK			
0008 736Fh	ICU	Interrupt Source Priority Register 111	IPR111	8	8	2 ICLK			Not available in 5-V packages.
0008 7372h	ICU	Interrupt Source Priority Register 114	IPR114	8	8	2 ICLK			
0008 7376h	ICU	Interrupt Source Priority Register 118	IPR118	8	8	2 ICLK			
0008 7379h	ICU	Interrupt Source Priority Register 121	IPR121	8	8	2 ICLK			
0008 737Bh	ICU	Interrupt Source Priority Register 123	IPR123	8	8	2 ICLK			
0008 737Dh	ICU	Interrupt Source Priority Register 125	IPR125	8	8	2 ICLK			
0008 737Fh	ICU	Interrupt Source Priority Register 127	IPR127	8	8	2 ICLK			
0008 7381h	ICU	Interrupt Source Priority Register 129	IPR129	8	8	2 ICLK			
0008 7385h	ICU	Interrupt Source Priority Register 133	IPR133	8	8	2 ICLK			
0008 7386h	ICU	Interrupt Source Priority Register 134	IPR134	8	8	2 ICLK			
0008 738Ah	ICU	Interrupt Source Priority Register 138	IPR138	8	8	2 ICLK			
0008 738Bh	ICU	Interrupt Source Priority Register 139	IPR139	8	8	2 ICLK			
0008 738Eh	ICU	Interrupt Source Priority Register 142	IPR142	8	8	2 ICLK			
0008 7392h	ICU	Interrupt Source Priority Register 146	IPR146	8	8	2 ICLK			
0008 7393h	ICU	Interrupt Source Priority Register 147	IPR147	8	8	2 ICLK			
0008 7395h	ICU	Interrupt Source Priority Register 149	IPR149	8	8	2 ICLK			
0008 7397h	ICU	Interrupt Source Priority Register 151	IPR151	8	8	2 ICLK			
0008 7399h	ICU	Interrupt Source Priority Register 153	IPR153	8	8	2 ICLK			
0008 739Bh	ICU	Interrupt Source Priority Register 155	IPR155	8	8	2 ICLK			
0008 739Fh	ICU	Interrupt Source Priority Register 159	IPR159	8	8	2 ICLK			
0008 73A0h	ICU	Interrupt Source Priority Register 160	IPR160	8	8	2 ICLK			
0008 73A2h	ICU	Interrupt Source Priority Register 162	IPR162	8	8	2 ICLK			
0008 73A4h	ICU	Interrupt Source Priority Register 164	IPR164	8	8	2 ICLK			
0008 73A6h	ICU	Interrupt Source Priority Register 166	IPR166	8	8	2 ICLK			
0008 73AAh	ICU	Interrupt Source Priority Register 170	IPR170	8	8	2 ICLK			
0008 73ABh	ICU	Interrupt Source Priority Register 171	IPR171	8	8	2 ICLK			
0008 73AEh	ICU	Interrupt Source Priority Register 174	IPR174	8	8	2 ICLK			
0008 73B1h	ICU	Interrupt Source Priority Register 177	IPR177	8	8	2 ICLK			
0008 73B4h	ICU	Interrupt Source Priority Register 180	IPR180	8	8	2 ICLK			
0008 73B7h	ICU	Interrupt Source Priority Register 183	IPR183	8	8	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (12 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 73BAh	ICU	Interrupt Source Priority Register 186	IPR186	8	8	2 ICLK		ICUb	
0008 73BEh	ICU	Interrupt Source Priority Register 190	IPR190	8	8	2 ICLK			
0008 73C2h	ICU	Interrupt Source Priority Register 194	IPR194	8	8	2 ICLK			
0008 73C6h	ICU	Interrupt Source Priority Register 198	IPR198	8	8	2 ICLK			
0008 73C7h	ICU	Interrupt Source Priority Register 199	IPR199	8	8	2 ICLK			
0008 73C8h	ICU	Interrupt Source Priority Register 200	IPR200	8	8	2 ICLK			
0008 73C9h	ICU	Interrupt Source Priority Register 201	IPR201	8	8	2 ICLK			
0008 73CAh	ICU	Interrupt Source Priority Register 202	IPR202	8	8	2 ICLK			
0008 73CBh	ICU	Interrupt Source Priority Register 203	IPR203	8	8	2 ICLK			
0008 73CCh	ICU	Interrupt Source Priority Register 204	IPR204	8	8	2 ICLK			
0008 73CDh	ICU	Interrupt Source Priority Register 205	IPR205	8	8	2 ICLK			
0008 73CEh	ICU	Interrupt Source Priority Register 206	IPR206	8	8	2 ICLK			
0008 73D2h	ICU	Interrupt Source Priority Register 210	IPR210	8	8	2 ICLK			
0008 73D6h	ICU	Interrupt Source Priority Register 214	IPR214	8	8	2 ICLK			
0008 73DAh	ICU	Interrupt Source Priority Register 218	IPR218	8	8	2 ICLK			
0008 73DEh	ICU	Interrupt Source Priority Register 222	IPR222	8	8	2 ICLK			
0008 73E2h	ICU	Interrupt Source Priority Register 226	IPR226	8	8	2 ICLK			
0008 73E6h	ICU	Interrupt Source Priority Register 230	IPR230	8	8	2 ICLK			
0008 73EAh	ICU	Interrupt Source Priority Register 234	IPR234	8	8	2 ICLK			
0008 73EEh	ICU	Interrupt Source Priority Register 238	IPR238	8	8	2 ICLK			
0008 73F2h	ICU	Interrupt Source Priority Register 242	IPR242	8	8	2 ICLK			
0008 73F3h	ICU	Interrupt Source Priority Register 243	IPR243	8	8	2 ICLK			
0008 73F4h	ICU	Interrupt Source Priority Register 244	IPR244	8	8	2 ICLK			
0008 73F5h	ICU	Interrupt Source Priority Register 245	IPR245	8	8	2 ICLK			
0008 73F6h	ICU	Interrupt Source Priority Register 246	IPR246	8	8	2 ICLK			
0008 73F7h	ICU	Interrupt Source Priority Register 247	IPR247	8	8	2 ICLK			
0008 73F8h	ICU	Interrupt Source Priority Register 248	IPR248	8	8	2 ICLK			
0008 73F9h	ICU	Interrupt Source Priority Register 249	IPR249	8	8	2 ICLK			
0008 73FAh	ICU	Interrupt Source Priority Register 250	IPR250	8	8	2 ICLK			
0008 7400h	ICU	DMAC Activation Request Select Register 0	DMRSR0	8	8	2 ICLK			
0008 7404h	ICU	DMAC Activation Request Select Register 1	DMRSR1	8	8	2 ICLK			
0008 7408h	ICU	DMAC Activation Request Select Register 2	DMRSR2	8	8	2 ICLK			
0008 740Ch	ICU	DMAC Activation Request Select Register 3	DMRSR3	8	8	2 ICLK			
0008 7500h	ICU	IRQ Control Register 0	IRQCR0	8	8	2 ICLK			
0008 7501h	ICU	IRQ Control Register 1	IRQCR1	8	8	2 ICLK			
0008 7502h	ICU	IRQ Control Register 2	IRQCR2	8	8	2 ICLK			
0008 7503h	ICU	IRQ Control Register 3	IRQCR3	8	8	2 ICLK			
0008 7504h	ICU	IRQ Control Register 4	IRQCR4	8	8	2 ICLK			
0008 7505h	ICU	IRQ Control Register 5	IRQCR5	8	8	2 ICLK			
0008 7506h	ICU	IRQ Control Register 6	IRQCR6	8	8	2 ICLK			
0008 7507h	ICU	IRQ Control Register 7	IRQCR7	8	8	2 ICLK			
0008 7508h	ICU	IRQ Control Register 8	IRQCR8	8	8	2 ICLK			
0008 7509h	ICU	IRQ Control Register 9	IRQCR9	8	8	2 ICLK			
0008 750Ah	ICU	IRQ Control Register 10	IRQCR10	8	8	2 ICLK			
0008 750Bh	ICU	IRQ Control Register 11	IRQCR11	8	8	2 ICLK			
0008 750Ch	ICU	IRQ Control Register 12	IRQCR12	8	8	2 ICLK			
0008 750Dh	CEC	CEC Interrupt Control Register 1	CECINTCR1	8	8	2 ICLK		CEC	Not available in 5-V packages.

Table 4.1 List of I/O Registers (Address Order) (13 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 750Eh	CEC	CEC Interrupt Control Register 2	CECINTCR2	8	8	2 ICLK		CEC	Not available in 5-V packages.
0008 750Fh	CEC	CEC Interrupt Control Register 3	CECINTCR3	8	8	2 ICLK			Not available in 5-V packages.
0008 7510h	ICU	IRQ Pin Digital Filter Enable Register 0	IRQFLTE0	8	8	2 ICLK		ICUb	
0008 7511h	ICU	IRQ Pin Digital Filter Enable Register 1	IRQFLTE1	8	8	2 ICLK			
0008 7514h	ICU	IRQ Pin Digital Filter Setting Register 0	IRQFLTC0	16	16	2 ICLK			
0008 7516h	ICU	IRQ Pin Digital Filter Setting Register 1	IRQFLTC1	16	16	2 ICLK			
0008 7580h	ICU	Non-Maskable Interrupt Status Register	NMISR	8	8	2 ICLK			
0008 7581h	ICU	Non-Maskable Interrupt Enable Register	NMIER	8	8	2 ICLK			
0008 7582h	ICU	Non-Maskable Interrupt Status Clear Register	NMICLR	8	8	2 ICLK			
0008 7583h	ICU	NMI Pin Interrupt Control Register	NMICR	8	8	2 ICLK			
0008 7590h	ICU	NMI Pin Digital Filter Enable Register	NMIFLTE	8	8	2 ICLK			
0008 7594h	ICU	NMI Pin Digital Filter Setting Register	NMIFLTC	8	8	2 ICLK			
0008 8000h	CMT	Compare Match Timer Start Register 0	CMSTR0	16	16	2 to 3PCLKB	2 ICLK	CMT	
0008 8002h	CMT0	Compare Match Timer Control Register	CMCR	16	16	2 to 3PCLKB	2 ICLK		
0008 8004h	CMT0	Compare Match Counter	CMCNT	16	16	2 to 3PCLKB	2 ICLK		
0008 8006h	CMT0	Compare Match Constant Register	CMCOR	16	16	2 to 3PCLKB	2 ICLK		
0008 8008h	CMT1	Compare Match Timer Control Register	CMCR	16	16	2 to 3PCLKB	2 ICLK		
0008 800Ah	CMT1	Compare Match Counter	CMCNT	16	16	2 to 3PCLKB	2 ICLK		
0008 800Ch	CMT1	Compare Match Constant Register	CMCOR	16	16	2 to 3PCLKB	2 ICLK		
0008 8010h	CMT	Compare Match Timer Start Register 1	CMSTR1	16	16	2 to 3PCLKB	2 ICLK		
0008 8012h	CMT2	Compare Match Timer Control Register	CMCR	16	16	2 to 3PCLKB	2 ICLK		
0008 8014h	CMT2	Compare Match Counter	CMCNT	16	16	2 to 3PCLKB	2 ICLK		
0008 8016h	CMT2	Compare Match Constant Register	CMCOR	16	16	2 to 3PCLKB	2 ICLK		
0008 8018h	CMT3	Compare Match Timer Control Register	CMCR	16	16	2 to 3PCLKB	2 ICLK		
0008 801Ah	CMT3	Compare Match Counter	CMCNT	16	16	2 to 3PCLKB	2 ICLK		
0008 801Ch	CMT3	Compare Match Constant Register	CMCOR	16	16	2 to 3PCLKB	2 ICLK		
0008 8020h	WDT	WDT Refresh Register	WDTRR	8	8	2 to 3PCLKB	2 ICLK	WDTA	
0008 8022h	WDT	WDT Control Register	WDTCR	16	16	2 to 3PCLKB	2 ICLK		
0008 8024h	WDT	WDT Status Register	WDTSR	16	16	2 to 3PCLKB	2 ICLK		
0008 8026h	WDT	WDT Reset Control Register	WDTRCR	8	8	2 to 3PCLKB	2 ICLK		
0008 8030h	IWDT	IWDT Refresh Register	IWDTRR	8	8	2 to 3PCLKB	2 ICLK	IWDTa	
0008 8032h	IWDT	IWDT Control Register	IWDTCR	16	16	2 to 3PCLKB	2 ICLK		
0008 8034h	IWDT	IWDT Status Register	IWDTSR	16	16	2 to 3PCLKB	2 ICLK		
0008 8036h	IWDT	IWDT Reset Control Register	IWDTRCR	8	8	2 to 3PCLKB	2 ICLK		
0008 8038h	IWDT	IWDT Count Stop Control Register	IWDTCSTPR	8	8	2 to 3PCLKB	2 ICLK		
0008 80C0h	DA	D/A Data Register 0	DADR0	16	16	2 to 3PCLKB	2 ICLK	DAa	
0008 80C2h	DA	D/A Data Register 1	DADR1	16	16	2 to 3PCLKB	2 ICLK		
0008 80C4h	DA	D/A Control Register	DACR	8	8	2 to 3PCLKB	2 ICLK		
0008 80C5h	DA	DADRm Format Select Register	DADPR	8	8	2 to 3PCLKB	2 ICLK		
0008 8100h	TPU	Timer Start Register	TSTR	8	8	2 to 3PCLKB	2 ICLK	TPUa	
0008 8101h	TPU	Timer Synchronous Register	TSYR	8	8	2 to 3PCLKB	2 ICLK		
0008 8108h	TPU0	Noise Filter Control Register	NFCR	8	8	2 to 3PCLKB	2 ICLK		
0008 8109h	TPU1	Noise Filter Control Register	NFCR	8	8	2 to 3PCLKB	2 ICLK		
0008 810Ah	TPU2	Noise Filter Control Register	NFCR	8	8	2 to 3PCLKB	2 ICLK		
0008 810Bh	TPU3	Noise Filter Control Register	NFCR	8	8	2 to 3PCLKB	2 ICLK		
0008 810Ch	TPU4	Noise Filter Control Register	NFCR	8	8	2 to 3PCLKB	2 ICLK		
0008 810Dh	TPU5	Noise Filter Control Register	NFCR	8	8	2 to 3PCLKB	2 ICLK		
0008 8110h	TPU0	Timer Control Register	TCR	8	8	2 to 3PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (14 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 8111h	TPU0	Timer Mode Register	TMDR	8	8	2 to 3PCLKB	2 ICLK	TPUa	
0008 8112h	TPU0	Timer I/O Control Register H	TIORH	8	8	2 to 3PCLKB	2 ICLK		
0008 8113h	TPU0	Timer I/O Control Register L	TIORL	8	8	2 to 3PCLKB	2 ICLK		
0008 8114h	TPU0	Timer Interrupt Enable Register	TIER	8	8	2 to 3PCLKB	2 ICLK		
0008 8115h	TPU0	Timer Status Register	TSR	8	8	2 to 3PCLKB	2 ICLK		
0008 8116h	TPU0	Timer Counter	TCNT	16	16	2 to 3PCLKB	2 ICLK		
0008 8118h	TPU0	Timer General Register A	TGRA	16	16	2 to 3PCLKB	2 ICLK		
0008 811Ah	TPU0	Timer General Register B	TGRB	16	16	2 to 3PCLKB	2 ICLK		
0008 811Ch	TPU0	Timer General Register C	TGRC	16	16	2 to 3PCLKB	2 ICLK		
0008 811Eh	TPU0	Timer General Register D	TGRD	16	16	2 to 3PCLKB	2 ICLK		
0008 8120h	TPU1	Timer Control Register	TCR	8	8	2 to 3PCLKB	2 ICLK		
0008 8121h	TPU1	Timer Mode Register	TMDR	8	8	2 to 3PCLKB	2 ICLK		
0008 8122h	TPU1	Timer I/O Control Register	TIOR	8	8	2 to 3PCLKB	2 ICLK		
0008 8124h	TPU1	Timer Interrupt Enable Register	TIER	8	8	2 to 3PCLKB	2 ICLK		
0008 8125h	TPU1	Timer Status Register	TSR	8	8	2 to 3PCLKB	2 ICLK		
0008 8126h	TPU1	Timer Counter	TCNT	16	16	2 to 3PCLKB	2 ICLK		
0008 8128h	TPU1	Timer General Register A	TGRA	16	16	2 to 3PCLKB	2 ICLK		
0008 812Ah	TPU1	Timer General Register B	TGRB	16	16	2 to 3PCLKB	2 ICLK		
0008 8130h	TPU2	Timer Control Register	TCR	8	8	2 to 3PCLKB	2 ICLK		
0008 8131h	TPU2	Timer Mode Register	TMDR	8	8	2 to 3PCLKB	2 ICLK		
0008 8132h	TPU2	Timer I/O Control Register	TIOR	8	8	2 to 3PCLKB	2 ICLK		
0008 8134h	TPU2	Timer Interrupt Enable Register	TIER	8	8	2 to 3PCLKB	2 ICLK		
0008 8135h	TPU2	Timer Status Register	TSR	8	8	2 to 3PCLKB	2 ICLK		
0008 8136h	TPU2	Timer Counter	TCNT	16	16	2 to 3PCLKB	2 ICLK		
0008 8138h	TPU2	Timer General Register A	TGRA	16	16	2 to 3PCLKB	2 ICLK		
0008 813Ah	TPU2	Timer General Register B	TGRB	16	16	2 to 3PCLKB	2 ICLK		
0008 8140h	TPU3	Timer Control Register	TCR	8	8	2 to 3PCLKB	2 ICLK		
0008 8141h	TPU3	Timer Mode Register	TMDR	8	8	2 to 3PCLKB	2 ICLK		
0008 8142h	TPU3	Timer I/O Control Register H	TIORH	8	8	2 to 3PCLKB	2 ICLK		
0008 8143h	TPU3	Timer I/O Control Register L	TIORL	8	8	2 to 3PCLKB	2 ICLK		
0008 8144h	TPU3	Timer Interrupt Enable Register	TIER	8	8	2 to 3PCLKB	2 ICLK		
0008 8145h	TPU3	Timer Status Register	TSR	8	8	2 to 3PCLKB	2 ICLK		
0008 8146h	TPU3	Timer Counter	TCNT	16	16	2 to 3PCLKB	2 ICLK		
0008 8148h	TPU3	Timer General Register A	TGRA	16	16	2 to 3PCLKB	2 ICLK		
0008 814Ah	TPU3	Timer General Register B	TGRB	16	16	2 to 3PCLKB	2 ICLK		
0008 814Ch	TPU3	Timer General Register C	TGRC	16	16	2 to 3PCLKB	2 ICLK		
0008 814Eh	TPU3	Timer General Register D	TGRD	16	16	2 to 3PCLKB	2 ICLK		
0008 8150h	TPU4	Timer Control Register	TCR	8	8	2 to 3PCLKB	2 ICLK		
0008 8151h	TPU4	Timer Mode Register	TMDR	8	8	2 to 3PCLKB	2 ICLK		
0008 8152h	TPU4	Timer I/O Control Register	TIOR	8	8	2 to 3PCLKB	2 ICLK		
0008 8154h	TPU4	Timer Interrupt Enable Register	TIER	8	8	2 to 3PCLKB	2 ICLK		
0008 8155h	TPU4	Timer Status Register	TSR	8	8	2 to 3PCLKB	2 ICLK		
0008 8156h	TPU4	Timer Counter	TCNT	16	16	2 to 3PCLKB	2 ICLK		
0008 8158h	TPU4	Timer General Register A	TGRA	16	16	2 to 3PCLKB	2 ICLK		
0008 815Ah	TPU4	Timer General Register B	TGRB	16	16	2 to 3PCLKB	2 ICLK		
0008 8160h	TPU5	Timer Control Register	TCR	8	8	2 to 3PCLKB	2 ICLK		
0008 8161h	TPU5	Timer Mode Register	TMDR	8	8	2 to 3PCLKB	2 ICLK		
0008 8162h	TPU5	Timer I/O Control Register	TIOR	8	8	2 to 3PCLKB	2 ICLK		
0008 8164h	TPU5	Timer Interrupt Enable Register	TIER	8	8	2 to 3PCLKB	2 ICLK		
0008 8165h	TPU5	Timer Status Register	TSR	8	8	2 to 3PCLKB	2 ICLK		
0008 8166h	TPU5	Timer Counter	TCNT	16	16	2 to 3PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (15 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 8168h	TPU5	Timer General Register A	TGRA	16	16	2 to 3PCLKB	2 ICLK	TPUa	
0008 816Ah	TPU5	Timer General Register B	TGRB	16	16	2 to 3PCLKB	2 ICLK		
0008 81E6h	PPG0	PPG Output Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK	PPG	
0008 81E7h	PPG0	PPG Output Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 81E8h	PPG0	Next Data Enable Registers H	NDERH	8	8	2 to 3PCLKB	2 ICLK		
0008 81E9h	PPG0	Next Data Enable Registers L	NDERL	8	8	2 to 3PCLKB	2 ICLK		
0008 81EAh	PPG0	Output Data Registers H	PODRH	8	8	2 to 3PCLKB	2 ICLK		
0008 81EBh	PPG0	Output Data Registers L	PODRL	8	8	2 to 3PCLKB	2 ICLK		
0008 81ECh	PPG0	Next Data Registers H	NDRH	8	8	2 to 3PCLKB	2 ICLK		
0008 81EDh	PPG0	Next Data Registers L	NDRL	8	8	2 to 3PCLKB	2 ICLK		
0008 81EEh	PPG0	Next Data Registers H	NDRH2	8	8	2 to 3PCLKB	2 ICLK		
0008 81EFh	PPG0	Next Data Registers L	NDRL2	8	8	2 to 3PCLKB	2 ICLK		
0008 8200h	TMR0	Timer Control Register	TCR	8	8	2 to 3PCLKB	2 ICLK	TMR	
0008 8201h	TMR1	Timer Control Register	TCR	8	8	2 to 3PCLKB	2 ICLK		
0008 8202h	TMR0	Timer Control/Status Register	TCSR	8	8	2 to 3PCLKB	2 ICLK		
0008 8203h	TMR1	Timer Control/Status Register	TCSR	8	8	2 to 3PCLKB	2 ICLK		
0008 8204h	TMR0	Time Constant Register A	TCORA	8	8	2 to 3PCLKB	2 ICLK		
0008 8205h	TMR1	Time Constant Register A	TCORA	8	8*1	2 to 3PCLKB	2 ICLK		
0008 8206h	TMR0	Time Constant Register B	TCORB	8	8	2 to 3PCLKB	2 ICLK		
0008 8207h	TMR1	Time Constant Register B	TCORB	8	8*1	2 to 3PCLKB	2 ICLK		
0008 8208h	TMR0	Timer Counter	TCNT	8	8	2 to 3PCLKB	2 ICLK		
0008 8209h	TMR1	Timer Counter	TCNT	8	8*1	2 to 3PCLKB	2 ICLK		
0008 820Ah	TMR0	Timer Counter Control Register	TCCR	8	8	2 to 3PCLKB	2 ICLK		
0008 820Bh	TMR1	Timer Counter Control Register	TCCR	8	8*1	2 to 3PCLKB	2 ICLK		
0008 820Ch	TMR0	Time Count Start Register	TCSTR	8	8	2 to 3PCLKB	2 ICLK		
0008 8210h	TMR2	Timer Control Register	TCR	8	8	2 to 3PCLKB	2 ICLK		
0008 8211h	TMR3	Timer Control Register	TCR	8	8	2 to 3PCLKB	2 ICLK		
0008 8212h	TMR2	Timer Control/Status Register	TCSR	8	8	2 to 3PCLKB	2 ICLK		
0008 8213h	TMR3	Timer Control/Status Register	TCSR	8	8	2 to 3PCLKB	2 ICLK		
0008 8214h	TMR2	Time Constant Register A	TCORA	8	8	2 to 3PCLKB	2 ICLK		
0008 8215h	TMR3	Time Constant Register A	TCORA	8	8*1	2 to 3PCLKB	2 ICLK		
0008 8216h	TMR2	Time Constant Register B	TCORB	8	8	2 to 3PCLKB	2 ICLK		
0008 8217h	TMR3	Time Constant Register B	TCORB	8	8*1	2 to 3PCLKB	2 ICLK		
0008 8218h	TMR2	Timer Counter	TCNT	8	8	2 to 3PCLKB	2 ICLK		
0008 8219h	TMR3	Timer Counter	TCNT	8	8*1	2 to 3PCLKB	2 ICLK		
0008 821Ah	TMR2	Timer Counter Control Register	TCCR	8	8	2 to 3PCLKB	2 ICLK		
0008 821Bh	TMR3	Timer Counter Control Register	TCCR	8	8*1	2 to 3PCLKB	2 ICLK		
0008 821Ch	TMR2	Time Count Start Register	TCSTR	8	8	2 to 3PCLKB	2 ICLK		
0008 8280h	CRC	CRC Control Register	CRCCR	8	8	2 to 3PCLKB	2 ICLK	CRC	
0008 8281h	CRC	CRC Data Input Register	CRCDIR	8	8	2 to 3PCLKB	2 ICLK		
0008 8282h	CRC	CRC Data Output Register	CRCDOR	16	16	2 to 3PCLKB	2 ICLK		
0008 8300h	RIIC0	I^2C Bus Control Register 1	ICCR1	8	8	2 to 3PCLKB	2 ICLK	RIIC	
0008 8301h	RIIC0	I^2C Bus Control Register 2	ICCR2	8	8	2 to 3PCLKB	2 ICLK		
0008 8302h	RIIC0	I^2C Bus Mode Register 1	ICMR1	8	8	2 to 3PCLKB	2 ICLK		
0008 8303h	RIIC0	I^2C Bus Mode Register 2	ICMR2	8	8	2 to 3PCLKB	2 ICLK		
0008 8304h	RIIC0	I^2C Bus Mode Register 3	ICMR3	8	8	2 to 3PCLKB	2 ICLK		
0008 8305h	RIIC0	I^2C Bus Function Enable Register	ICFER	8	8	2 to 3PCLKB	2 ICLK		
0008 8306h	RIIC0	I^2C Bus Status Enable Register	ICSER	8	8	2 to 3PCLKB	2 ICLK		
0008 8307h	RIIC0	I^2C Bus Interrupt Enable Register	ICIER	8	8	2 to 3PCLKB	2 ICLK		
0008 8308h	RIIC0	I^2C Bus Status Register 1	ICSR1	8	8	2 to 3PCLKB	2 ICLK		
0008 8309h	RIIC0	I^2C Bus Status Register 2	ICSR2	8	8	2 to 3PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (16 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 830Ah	RIIC0	Slave Address Register L0	SARL0	8	8	2 to 3PCLKB	2 ICLK	RIIC	
0008 830Ah	RIIC0	Timeout Internal Counter L	TMOCNTL	8	8	2 to 3PCLKB	2 ICLK		
0008 830Bh	RIIC0	Slave Address Register U0	SARU0	8	8	2 to 3PCLKB	2 ICLK		
0008 830Bh	RIIC0	Timeout Internal Counter U	TMOCNTU	8	8*2	2 to 3PCLKB	2 ICLK		
0008 830Ch	RIIC0	Slave Address Register L1	SARL1	8	8	2 to 3PCLKB	2 ICLK		
0008 830Dh	RIIC0	Slave Address Register U1	SARU1	8	8	2 to 3PCLKB	2 ICLK		
0008 830Eh	RIIC0	Slave Address Register L2	SARL2	8	8	2 to 3PCLKB	2 ICLK		
0008 830Fh	RIIC0	Slave Address Register U2	SARU2	8	8	2 to 3PCLKB	2 ICLK		
0008 8310h	RIIC0	I2C Bus Bit Rate Low-Level Register	ICBRL	8	8	2 to 3PCLKB	2 ICLK		
0008 8311h	RIIC0	I2C Bus Bit Rate High-Level Register	ICBRH	8	8	2 to 3PCLKB	2 ICLK		
0008 8312h	RIIC0	I2C Bus Transmit Data Register	ICDRT	8	8	2 to 3PCLKB	2 ICLK		
0008 8313h	RIIC0	I2C Bus Receive Data Register	ICDRR	8	8	2 to 3PCLKB	2 ICLK		
0008 8320h	RIIC1	I2C Bus Control Register 1	ICCR1	8	8	2 to 3PCLKB	2 ICLK		
0008 8321h	RIIC1	I2C Bus Control Register 2	ICCR2	8	8	2 to 3PCLKB	2 ICLK		
0008 8322h	RIIC1	I2C Bus Mode Register 1	ICMR1	8	8	2 to 3PCLKB	2 ICLK		
0008 8323h	RIIC1	I2C Bus Mode Register 2	ICMR2	8	8	2 to 3PCLKB	2 ICLK		
0008 8324h	RIIC1	I2C Bus Mode Register 3	ICMR3	8	8	2 to 3PCLKB	2 ICLK		
0008 8325h	RIIC1	I2C Bus Function Enable Register	ICFER	8	8	2 to 3PCLKB	2 ICLK		
0008 8326h	RIIC1	I2C Bus Status Enable Register	ICSER	8	8	2 to 3PCLKB	2 ICLK		
0008 8327h	RIIC1	I2C Bus Interrupt Enable Register	ICIER	8	8	2 to 3PCLKB	2 ICLK		
0008 8328h	RIIC1	I2C Bus Status Register 1	ICSR1	8	8	2 to 3PCLKB	2 ICLK		
0008 8329h	RIIC1	I2C Bus Status Register 2	ICSR2	8	8	2 to 3PCLKB	2 ICLK		
0008 832Ah	RIIC1	Slave Address Register L0	SARL0	8	8	2 to 3PCLKB	2 ICLK		
0008 832Ah	RIIC1	Timeout Internal Counter L	TMOCNTL	8	8	2 to 3PCLKB	2 ICLK		
0008 832Bh	RIIC1	Slave Address Register U0	SARU0	8	8	2 to 3PCLKB	2 ICLK		
0008 832Bh	RIIC1	Timeout Internal Counter U	TMOCNTU	8	8*2	2 to 3PCLKB	2 ICLK		
0008 832Ch	RIIC1	Slave Address Register L1	SARL1	8	8	2 to 3PCLKB	2 ICLK		
0008 832Dh	RIIC1	Slave Address Register U1	SARU1	8	8	2 to 3PCLKB	2 ICLK		
0008 832Eh	RIIC1	Slave Address Register L2	SARL2	8	8	2 to 3PCLKB	2 ICLK		
0008 832Fh	RIIC1	Slave Address Register U2	SARU2	8	8	2 to 3PCLKB	2 ICLK		
0008 8330h	RIIC1	I2C Bus Bit Rate Low-Level Register	ICBRL	8	8	2 to 3PCLKB	2 ICLK		
0008 8331h	RIIC1	I2C Bus Bit Rate High-Level Register	ICBRH	8	8	2 to 3PCLKB	2 ICLK		
0008 8332h	RIIC1	I2C Bus Transmit Data Register	ICDRT	8	8	2 to 3PCLKB	2 ICLK		
0008 8333h	RIIC1	I2C Bus Receive Data Register	ICDRR	8	8	2 to 3PCLKB	2 ICLK		
0008 8360h	RIIC3	I2C Bus Control Register 1	ICCR1	8	8	2 to 3PCLKB	2 ICLK		
0008 8361h	RIIC3	I2C Bus Control Register 2	ICCR2	8	8	2 to 3PCLKB	2 ICLK		
0008 8362h	RIIC3	I2C Bus Mode Register 1	ICMR1	8	8	2 to 3PCLKB	2 ICLK		
0008 8363h	RIIC3	I2C Bus Mode Register 2	ICMR2	8	8	2 to 3PCLKB	2 ICLK		
0008 8364h	RIIC3	I2C Bus Mode Register 3	ICMR3	8	8	2 to 3PCLKB	2 ICLK		
0008 8365h	RIIC3	I2C Bus Function Enable Register	ICFER	8	8	2 to 3PCLKB	2 ICLK		
0008 8366h	RIIC3	I2C Bus Status Enable Register	ICSER	8	8	2 to 3PCLKB	2 ICLK		
0008 8367h	RIIC3	I2C Bus Interrupt Enable Register	ICIER	8	8	2 to 3PCLKB	2 ICLK		
0008 8368h	RIIC3	I2C Bus Status Register 1	ICSR1	8	8	2 to 3PCLKB	2 ICLK		
0008 8369h	RIIC3	I2C Bus Status Register 2	ICSR2	8	8	2 to 3PCLKB	2 ICLK		
0008 836Ah	RIIC3	Slave Address Register L0	SARL0	8	8	2 to 3PCLKB	2 ICLK		
0008 836Ah	RIIC3	Timeout Internal Counter L	TMOCNTL	8	8	2 to 3PCLKB	2 ICLK		
0008 836Bh	RIIC3	Slave Address Register U0	SARU0	8	8	2 to 3PCLKB	2 ICLK		
0008 836Bh	RIIC3	Timeout Internal Counter U	TMOCNTU	8	8*2	2 to 3PCLKB	2 ICLK		
0008 836Ch	RIIC3	Slave Address Register L1	SARL1	8	8	2 to 3PCLKB	2 ICLK		
0008 836Dh	RIIC3	Slave Address Register U1	SARU1	8	8	2 to 3PCLKB	2 ICLK		
0008 836Eh	RIIC3	Slave Address Register L2	SARL2	8	8	2 to 3PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (17 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 836Fh	RIIC3	Slave Address Register U2	SARU2	8	8	2 to 3PCLKB	2 ICLK	RIIC	
0008 8370h	RIIC3	I²C Bus Bit Rate Low-Level Register	ICBRL	8	8	2 to 3PCLKB	2 ICLK		
0008 8371h	RIIC3	I²C Bus Bit Rate High-Level Register	ICBRH	8	8	2 to 3PCLKB	2 ICLK		
0008 8372h	RIIC3	I²C Bus Transmit Data Register	ICDRT	8	8	2 to 3PCLKB	2 ICLK		
0008 8373h	RIIC3	I²C Bus Receive Data Register	ICDRR	8	8	2 to 3PCLKB	2 ICLK		
0008 8380h	RSPI0	RSPI Control Register	SPCR	8	8	2 to 3PCLKB	2 ICLK	RSPI	
0008 8381h	RSPI0	RSPI Slave Select Polarity Register	SSLP	8	8	2 to 3PCLKB	2 ICLK		
0008 8382h	RSPI0	RSPI Pin Control Register	SPPCR	8	8	2 to 3PCLKB	2 ICLK		
0008 8383h	RSPI0	RSPI Status Register	SPSR	8	8	2 to 3PCLKB	2 ICLK		
0008 8384h	RSPI0	RSPI Data Register	SPDR	32	16, 32	2 to 3PCLKB	2 ICLK		
0008 8388h	RSPI0	RSPI Sequence Control Register	SPSCR	8	8	2 to 3PCLKB	2 ICLK		
0008 8389h	RSPI0	RSPI Sequence Status Register	SPSSR	8	8	2 to 3PCLKB	2 ICLK		
0008 838Ah	RSPI0	RSPI Bit Rate Register	SPBR	8	8	2 to 3PCLKB	2 ICLK		
0008 838Bh	RSPI0	RSPI Data Control Register	SPDCR	8	8	2 to 3PCLKB	2 ICLK		
0008 838Ch	RSPI0	RSPI Clock Delay Register	SPCKD	8	8	2 to 3PCLKB	2 ICLK		
0008 838Dh	RSPI0	RSPI Slave Select Negation Delay Register	SSLND	8	8	2 to 3PCLKB	2 ICLK		
0008 838Eh	RSPI0	RSPI Next-Access Delay Register	SPND	8	8	2 to 3PCLKB	2 ICLK		
0008 838Fh	RSPI0	RSPI Control Register 2	SPCR2	8	8	2 to 3PCLKB	2 ICLK		
0008 8390h	RSPI0	RSPI Command Register 0	SPCMD0	16	16	2 to 3PCLKB	2 ICLK		
0008 8392h	RSPI0	RSPI Command Register 1	SPCMD1	16	16	2 to 3PCLKB	2 ICLK		
0008 8394h	RSPI0	RSPI Command Register 2	SPCMD2	16	16	2 to 3PCLKB	2 ICLK		
0008 8396h	RSPI0	RSPI Command Register 3	SPCMD3	16	16	2 to 3PCLKB	2 ICLK		
0008 8398h	RSPI0	RSPI Command Register 4	SPCMD4	16	16	2 to 3PCLKB	2 ICLK		
0008 839Ah	RSPI0	RSPI Command Register 5	SPCMD5	16	16	2 to 3PCLKB	2 ICLK		
0008 839Ch	RSPI0	RSPI Command Register 6	SPCMD6	16	16	2 to 3PCLKB	2 ICLK		
0008 839Eh	RSPI0	RSPI Command Register 7	SPCMD7	16	16	2 to 3PCLKB	2 ICLK		
0008 83A0h	RSPI1	RSPI Control Register	SPCR	8	8	2 to 3PCLKB	2 ICLK		
0008 83A1h	RSPI1	RSPI Slave Select Polarity Register	SSLP	8	8	2 to 3PCLKB	2 ICLK		
0008 83A2h	RSPI1	RSPI Pin Control Register	SPPCR	8	8	2 to 3PCLKB	2 ICLK		
0008 83A3h	RSPI1	RSPI Status Register	SPSR	8	8	2 to 3PCLKB	2 ICLK		
0008 83A4h	RSPI1	RSPI Data Register	SPDR	32	16, 32	2 to 3PCLKB	2 ICLK		
0008 83A8h	RSPI1	RSPI Sequence Control Register	SPSCR	8	8	2 to 3PCLKB	2 ICLK		
0008 83A9h	RSPI1	RSPI Sequence Status Register	SPSSR	8	8	2 to 3PCLKB	2 ICLK		
0008 83AAh	RSPI1	RSPI Bit Rate Register	SPBR	8	8	2 to 3PCLKB	2 ICLK		
0008 83ABh	RSPI1	RSPI Data Control Register	SPDCR	8	8	2 to 3PCLKB	2 ICLK		
0008 83ACh	RSPI1	RSPI Clock Delay Register	SPCKD	8	8	2 to 3PCLKB	2 ICLK		
0008 83ADh	RSPI1	RSPI Slave Select Negation Delay Register	SSLND	8	8	2 to 3PCLKB	2 ICLK		
0008 83AEh	RSPI1	RSPI Next-Access Delay Register	SPND	8	8	2 to 3PCLKB	2 ICLK		
0008 83AFh	RSPI1	RSPI Control Register 2	SPCR2	8	8	2 to 3PCLKB	2 ICLK		
0008 83B0h	RSPI1	RSPI Command Register 0	SPCMD0	16	16	2 to 3PCLKB	2 ICLK		
0008 83B2h	RSPI1	RSPI Command Register 1	SPCMD1	16	16	2 to 3PCLKB	2 ICLK		
0008 83B4h	RSPI1	RSPI Command Register 2	SPCMD2	16	16	2 to 3PCLKB	2 ICLK		
0008 83B6h	RSPI1	RSPI Command Register 3	SPCMD3	16	16	2 to 3PCLKB	2 ICLK		
0008 83B8h	RSPI1	RSPI Command Register 4	SPCMD4	16	16	2 to 3PCLKB	2 ICLK		
0008 83BAh	RSPI1	RSPI Command Register 5	SPCMD5	16	16	2 to 3PCLKB	2 ICLK		
0008 83BCh	RSPI1	RSPI Command Register 6	SPCMD6	16	16	2 to 3PCLKB	2 ICLK		
0008 83BEh	RSPI1	RSPI Command Register 7	SPCMD7	16	16	2 to 3PCLKB	2 ICLK		
0008 8600h	MTU3	Timer Control Register	TCR	8	8	2 to 3PCLKB	2 ICLK	MTU2a	
0008 8601h	MTU4	Timer Control Register	TCR	8	8	2 to 3PCLKB	2 ICLK		
0008 8602h	MTU3	Timer Mode Register	TMDR	8	8	2 to 3PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (18 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 8603h	MTU4	Timer Mode Register	TMDR	8	8	2 to 3PCLKB	2 ICLK	MTU2a	
0008 8604h	MTU3	Timer I/O Control Register H	TIORH	8	8	2 to 3PCLKB	2 ICLK		
0008 8605h	MTU3	Timer I/O Control Register L	TIORL	8	8	2 to 3PCLKB	2 ICLK		
0008 8606h	MTU4	Timer I/O Control Register H	TIORH	8	8	2 to 3PCLKB	2 ICLK		
0008 8607h	MTU4	Timer I/O Control Register L	TIORL	8	8	2 to 3PCLKB	2 ICLK		
0008 8608h	MTU3	Timer Interrupt Enable Register	TIER	8	8	2 to 3PCLKB	2 ICLK		
0008 8609h	MTU4	Timer Interrupt Enable Register	TIER	8	8	2 to 3PCLKB	2 ICLK		
0008 860Ah	MTU	Timer Output Master Enable Register	TOER	8	8	2 to 3PCLKB	2 ICLK		
0008 860Dh	MTU	Timer Gate Control Register	TGCR	8	8	2 to 3PCLKB	2 ICLK		
0008 860Eh	MTU	Timer Output Control Register 1	TOCR1	8	8	2 to 3PCLKB	2 ICLK		
0008 860Fh	MTU	Timer Output Control Register 2	TOCR2	8	8	2 to 3PCLKB	2 ICLK		
0008 8610h	MTU3	Timer Counter	TCNT	16	16	2 to 3PCLKB	2 ICLK		
0008 8612h	MTU4	Timer Counter	TCNT	16	16	2 to 3PCLKB	2 ICLK		
0008 8614h	MTU	Timer Cycle Data Register	TCDR	16	16	2 to 3PCLKB	2 ICLK		
0008 8616h	MTU	Timer Dead Time Data Register	TDDR	16	16	2 to 3PCLKB	2 ICLK		
0008 8618h	MTU3	Timer General Register A	TGRA	16	16	2 to 3PCLKB	2 ICLK		
0008 861Ah	MTU3	Timer General Register B	TGRB	16	16	2 to 3PCLKB	2 ICLK		
0008 861Ch	MTU4	Timer General Register A	TGRA	16	16	2 to 3PCLKB	2 ICLK		
0008 861Eh	MTU4	Timer General Register B	TGRB	16	16	2 to 3PCLKB	2 ICLK		
0008 8620h	MTU	Timer Subcounter	TCNTS	16	16	2 to 3PCLKB	2 ICLK		
0008 8622h	MTU	Timer Cycle Buffer Register	TCBR	16	16	2 to 3PCLKB	2 ICLK		
0008 8624h	MTU3	Timer General Register C	TGRC	16	16	2 to 3PCLKB	2 ICLK		
0008 8626h	MTU3	Timer General Register D	TGRD	16	16	2 to 3PCLKB	2 ICLK		
0008 8628h	MTU4	Timer General Register C	TGRC	16	16	2 to 3PCLKB	2 ICLK		
0008 862Ah	MTU4	Timer General Register D	TGRD	16	16	2 to 3PCLKB	2 ICLK		
0008 862Ch	MTU3	Timer Status Register	TSR	8	8	2 to 3PCLKB	2 ICLK		
0008 862Dh	MTU4	Timer Status Register	TSR	8	8	2 to 3PCLKB	2 ICLK		
0008 8630h	MTU	Timer Interrupt Skipping Set Register	TITCR	8	8	2 to 3PCLKB	2 ICLK		
0008 8631h	MTU	Timer Interrupt Skipping Counter	TITCNT	8	8	2 to 3PCLKB	2 ICLK		
0008 8632h	MTU	Timer Buffer Transfer Set Register	TBTER	8	8	2 to 3PCLKB	2 ICLK		
0008 8634h	MTU	Timer Dead Time Enable Register	TDER	8	8	2 to 3PCLKB	2 ICLK		
0008 8636h	MTU	Timer Output Level Buffer Register	TOLBR	8	8	2 to 3PCLKB	2 ICLK		
0008 8638h	MTU3	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	2 to 3PCLKB	2 ICLK		
0008 8639h	MTU4	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	2 to 3PCLKB	2 ICLK		
0008 8640h	MTU4	Timer A/D Converter Start Request Control Register	TADCR	16	16	2 to 3PCLKB	2 ICLK		
0008 8644h	MTU4	Timer A/D Converter Start Request Cycle Set Register A	TADCORA	16	16	2 to 3PCLKB	2 ICLK		
0008 8646h	MTU4	Timer A/D Converter Start Request Cycle Set Register B	TADCORB	16	16	2 to 3PCLKB	2 ICLK		
0008 8648h	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register A	TADCOBRA	16	16	2 to 3PCLKB	2 ICLK		
0008 864Ah	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register B	TADCOBRB	16	16	2 to 3PCLKB	2 ICLK		
0008 8660h	MTU	Timer Waveform Control Register	TWCR	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 8680h	MTU	Timer Start Register	TSTR	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 8681h	MTU	Timer Synchronous Register	TSYR	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 8684h	MTU	Timer Read/Write Enable Register	TRWER	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 8690h	MTU0	Noise Filter Control Register	NFCR	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 8691h	MTU1	Noise Filter Control Register	NFCR	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 8692h	MTU2	Noise Filter Control Register	NFCR	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 8693h	MTU3	Noise Filter Control Register	NFCR	8	8, 16	2 to 3PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (19 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 8694h	MTU4	Noise Filter Control Register	NFCR	8	8, 16	2 to 3PCLKB	2 ICLK	MTU2a	
0008 8695h	MTU5	Noise Filter Control Register	NFCR	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 8700h	MTU0	Timer Control Register	TCR	8	8	2 to 3PCLKB	2 ICLK		
0008 8701h	MTU0	Timer Mode Register	TMDR	8	8	2 to 3PCLKB	2 ICLK		
0008 8702h	MTU0	Timer I/O Control Register H	TIORH	8	8	2 to 3PCLKB	2 ICLK		
0008 8703h	MTU0	Timer I/O Control Register L	TIORL	8	8	2 to 3PCLKB	2 ICLK		
0008 8704h	MTU0	Timer Interrupt Enable Register	TIER	8	8	2 to 3PCLKB	2 ICLK		
0008 8705h	MTU0	Timer Status Register	TSR	8	8	2 to 3PCLKB	2 ICLK		
0008 8706h	MTU0	Timer Counter	TCNT	16	16	2 to 3PCLKB	2 ICLK		
0008 8708h	MTU0	Timer General Register A	TGRA	16	16	2 to 3PCLKB	2 ICLK		
0008 870Ah	MTU0	Timer General Register B	TGRB	16	16	2 to 3PCLKB	2 ICLK		
0008 870Ch	MTU0	Timer General Register C	TGRC	16	16	2 to 3PCLKB	2 ICLK		
0008 870Eh	MTU0	Timer General Register D	TGRD	16	16	2 to 3PCLKB	2 ICLK		
0008 8720h	MTU0	Timer General Register E	TGRE	16	16	2 to 3PCLKB	2 ICLK		
0008 8722h	MTU0	Timer General Register F	TGRF	16	16	2 to 3PCLKB	2 ICLK		
0008 8724h	MTU0	Timer Interrupt Enable Register 2	TIER2	8	8	2 to 3PCLKB	2 ICLK		
0008 8726h	MTU0	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	2 to 3PCLKB	2 ICLK		
0008 8780h	MTU1	Timer Control Register	TCR	8	8	2 to 3PCLKB	2 ICLK		
0008 8781h	MTU1	Timer Mode Register	TMDR	8	8	2 to 3PCLKB	2 ICLK		
0008 8782h	MTU1	Timer I/O Control Register	TIOR	8	8	2 to 3PCLKB	2 ICLK		
0008 8784h	MTU1	Timer Interrupt Enable Register	TIER	8	8	2 to 3PCLKB	2 ICLK		
0008 8785h	MTU1	Timer Status Register	TSR	8	8	2 to 3PCLKB	2 ICLK		
0008 8786h	MTU1	Timer Counter	TCNT	16	16	2 to 3PCLKB	2 ICLK		
0008 8788h	MTU1	Timer General Register A	TGRA	16	16	2 to 3PCLKB	2 ICLK		
0008 878Ah	MTU1	Timer General Register B	TGRB	16	16	2 to 3PCLKB	2 ICLK		
0008 8790h	MTU1	Timer Input Capture Control Register	TICCR	8	8	2 to 3PCLKB	2 ICLK		
0008 8800h	MTU2	Timer Control Register	TCR	8	8	2 to 3PCLKB	2 ICLK		
0008 8801h	MTU2	Timer Mode Register	TMDR	8	8	2 to 3PCLKB	2 ICLK		
0008 8802h	MTU2	Timer I/O Control Register	TIOR	8	8	2 to 3PCLKB	2 ICLK		
0008 8804h	MTU2	Timer Interrupt Enable Register	TIER	8	8	2 to 3PCLKB	2 ICLK		
0008 8805h	MTU2	Timer Status Register	TSR	8	8	2 to 3PCLKB	2 ICLK		
0008 8806h	MTU2	Timer Counter	TCNT	16	16	2 to 3PCLKB	2 ICLK		
0008 8808h	MTU2	Timer General Register A	TGRA	16	16	2 to 3PCLKB	2 ICLK		
0008 880Ah	MTU2	Timer General Register B	TGRB	16	16	2 to 3PCLKB	2 ICLK		
0008 8880h	MTU5	Timer Counter U	TCNTU	16	16	2 to 3PCLKB	2 ICLK		
0008 8882h	MTU5	Timer General Register U	TGRU	16	16	2 to 3PCLKB	2 ICLK		
0008 8884h	MTU5	Timer Control Register U	TCRU	8	8	2 to 3PCLKB	2 ICLK		
0008 8886h	MTU5	Timer I/O Control Register U	TIORU	8	8	2 to 3PCLKB	2 ICLK		
0008 8890h	MTU5	Timer Counter V	TCNTV	16	16	2 to 3PCLKB	2 ICLK		
0008 8892h	MTU5	Timer General Register V	TGRV	16	16	2 to 3PCLKB	2 ICLK		
0008 8894h	MTU5	Timer Control Register V	TCRV	8	8	2 to 3PCLKB	2 ICLK		
0008 8896h	MTU5	Timer I/O Control Register V	TIORV	8	8	2 to 3PCLKB	2 ICLK		
0008 88A0h	MTU5	Timer Counter W	TCNTW	16	16	2 to 3PCLKB	2 ICLK		
0008 88A2h	MTU5	Timer General Register W	TGRW	16	16	2 to 3PCLKB	2 ICLK		
0008 88A4h	MTU5	Timer Control Register W	TCRW	8	8	2 to 3PCLKB	2 ICLK		
0008 88A6h	MTU5	Timer I/O Control Register W	TIORW	8	8	2 to 3PCLKB	2 ICLK		
0008 88B2h	MTU5	Timer Interrupt Enable Register	TIER	8	8	2 to 3PCLKB	2 ICLK		
0008 88B4h	MTU5	Timer Start Register	TSTR	8	8	2 to 3PCLKB	2 ICLK		
0008 88B6h	MTU5	Timer Compare Match Clear Register	TCNTCMPCLR	8	8	2 to 3PCLKB	2 ICLK		
0008 8900h	POE	Input Level Control/Status Register 1	ICSR1	16	16	2 to 3PCLKB	2 ICLK	POE2a	
0008 8902h	POE	Output Level Control/Status Register 1	OCSR1	16	16	2 to 3PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (20 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 8908h	POE	Input Level Control/Status Register 2	ICSR2	16	16	2 to 3PCLKB	2 ICLK	POE2a	
0008 890Ah	POE	Software Port Output Enable Register	SPOER	8	8	2 to 3PCLKB	2 ICLK		
0008 890Bh	POE	Port Output Enable Control Register 1	POECR1	8	8	2 to 3PCLKB	2 ICLK		
0008 890Ch	POE	Port Output Enable Control Register 2	POECR2	8	8	2 to 3PCLKB	2 ICLK		
0008 890Eh	POE	Input Level Control/Status Register 3	ICSR3	16	16	2 to 3PCLKB	2 ICLK		
0008 9000h	S12AD	A/D Control Register	ADCSR	16	16	2 to 3PCLKB	2 ICLK	S12ADB	
0008 9004h	S12AD	A/D Channel Select Register A	ADANSA	16	16	2 to 3PCLKB	2 ICLK		
0008 9008h	S12AD	A/D-Converted Value Addition Mode Select Register	ADADS	16	16	2 to 3PCLKB	2 ICLK		
0008 900Ch	S12AD	A/D-Converted Value Addition Count Select Register	ADADC	8	8	2 to 3PCLKB	2 ICLK		
0008 900Eh	S12AD	A/D Control Extended Register	ADCER	16	16	2 to 3PCLKB	2 ICLK		
0008 9010h	S12AD	A/D Start Trigger Select Register	ADSTRGR	16	16	2 to 3PCLKB	2 ICLK		
0008 9012h	S12AD	A/D Conversion Extended Input Control Register	ADEXICR	16	16	2 to 3PCLKB	2 ICLK		
0008 9014h	S12AD	A/D Channel Select Register B	ADANSB	16	16	2 to 3PCLKB	2 ICLK		
0008 9018h	S12AD	A/D Data-Doubling Register	ADDBLDR	16	16	2 to 3PCLKB	2 ICLK		
0008 901Ch	S12AD	A/D Internal Reference Voltage Data Register	ADOCDR	16	16	2 to 3PCLKB	2 ICLK		
0008 901Eh	S12AD	A/D Self-Diagnosis Data Register	ADRD	16	16	2 to 3PCLKB	2 ICLK		
0008 9020h	S12AD	A/D Data Registers 0	ADDR0	16	16	2 to 3PCLKB	2 ICLK		
0008 9022h	S12AD	A/D Data Registers 1	ADDR1	16	16	2 to 3PCLKB	2 ICLK		
0008 9024h	S12AD	A/D Data Registers 2	ADDR2	16	16	2 to 3PCLKB	2 ICLK		
0008 9026h	S12AD	A/D Data Registers 3	ADDR3	16	16	2 to 3PCLKB	2 ICLK		
0008 9028h	S12AD	A/D Data Registers 4	ADDR4	16	16	2 to 3PCLKB	2 ICLK		
0008 902Ah	S12AD	A/D Data Registers 5	ADDR5	16	16	2 to 3PCLKB	2 ICLK		
0008 902Ch	S12AD	A/D Data Registers 6	ADDR6	16	16	2 to 3PCLKB	2 ICLK		
0008 902Eh	S12AD	A/D Data Registers 7	ADDR7	16	16	2 to 3PCLKB	2 ICLK		
0008 9030h	S12AD	A/D Data Registers 8	ADDR8	16	16	2 to 3PCLKB	2 ICLK		
0008 9032h	S12AD	A/D Data Registers 9	ADDR9	16	16	2 to 3PCLKB	2 ICLK		
0008 9034h	S12AD	A/D Data Registers 10	ADDR10	16	16	2 to 3PCLKB	2 ICLK		
0008 9036h	S12AD	A/D Data Registers 11	ADDR11	16	16	2 to 3PCLKB	2 ICLK		
0008 9038h	S12AD	A/D Data Registers 12	ADDR12	16	16	2 to 3PCLKB	2 ICLK		
0008 903Ah	S12AD	A/D Data Registers 13	ADDR13	16	16	2 to 3PCLKB	2 ICLK		
0008 903Ch	S12AD	A/D Data Registers 14	ADDR14	16	16	2 to 3PCLKB	2 ICLK		
0008 903Eh	S12AD	A/D Data Registers 15	ADDR15	16	16	2 to 3PCLKB	2 ICLK		
0008 9060h	S12AD	A/D Sampling State Register 0	ADSSTR0	8	8	2 to 3PCLKB	2 ICLK		
0008 9061h	S12AD	A/D Sampling State Register L	ADSSTRL	8	8	2 to 3PCLKB	2 ICLK		
0008 9066h	S12AD	A/D Sample and Hold Circuit Control Register	ADSHCR	16	16	2 to 3PCLKB	2 ICLK		
0008 9071h	S12AD	A/D Sampling State Register O	ADSSTRO	8	8	2 to 3PCLKB	2 ICLK		
0008 9073h	S12AD	A/D Sampling State Register 1	ADSSTR1	8	8	2 to 3PCLKB	2 ICLK		
0008 9074h	S12AD	A/D Sampling State Register 2	ADSSTR2	8	8	2 to 3PCLKB	2 ICLK		
0008 9075h	S12AD	A/D Sampling State Register 3	ADSSTR3	8	8	2 to 3PCLKB	2 ICLK		
0008 9076h	S12AD	A/D Sampling State Register 4	ADSSTR4	8	8	2 to 3PCLKB	2 ICLK		
0008 9077h	S12AD	A/D Sampling State Register 5	ADSSTR5	8	8	2 to 3PCLKB	2 ICLK		
0008 9078h	S12AD	A/D Sampling State Register 6	ADSSTR6	8	8	2 to 3PCLKB	2 ICLK		
0008 9079h	S12AD	A/D Sampling State Register 7	ADSSTR7	8	8	2 to 3PCLKB	2 ICLK		
0008 907Ah	S12AD	A/D Disconnecting Detection Control Register	ADDISCR	8	8	2 to 3PCLKB	2 ICLK		
0008 A000h	SCI0	Serial Mode Register	SMR	8	8	2 to 3PCLKB	2 ICLK	SCIe, SCIf	
0008 A001h	SCI0	Bit Rate Register	BRR	8	8	2 to 3PCLKB	2 ICLK		
0008 A002h	SCI0	Serial Control Register	SCR	8	8	2 to 3PCLKB	2 ICLK		
0008 A003h	SCI0	Transmit Data Register	TDR	8	8	2 to 3PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (21 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 A004h	SCI0	Serial Status Register	SSR	8	8	2 to 3PCLKB	2 ICLK	SCIe, SCIf	
0008 A005h	SCI0	Receive Data Register	RDR	8	8	2 to 3PCLKB	2 ICLK		
0008 A006h	SCI0	Smart Card Mode Register	SCMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A007h	SCI0	Serial Extended Mode Register	SEMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A008h	SCI0	Noise Filter Setting Register	SNFR	8	8	2 to 3PCLKB	2 ICLK		
0008 A009h	SCI0	I^2C Mode Register 1	SIMR1	8	8	2 to 3PCLKB	2 ICLK		
0008 A00Ah	SCI0	I^2C Mode Register 2	SIMR2	8	8	2 to 3PCLKB	2 ICLK		
0008 A00Bh	SCI0	I^2C Mode Register 3	SIMR3	8	8	2 to 3PCLKB	2 ICLK		
0008 A00Ch	SCI0	I^2C Status Register	SISR	8	8	2 to 3PCLKB	2 ICLK		
0008 A00Dh	SCI0	SPI Mode Register	SPMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A020h	SCI1	Serial Mode Register	SMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A021h	SCI1	Bit Rate Register	BRR	8	8	2 to 3PCLKB	2 ICLK		
0008 A022h	SCI1	Serial Control Register	SCR	8	8	2 to 3PCLKB	2 ICLK		
0008 A023h	SCI1	Transmit Data Register	TDR	8	8	2 to 3PCLKB	2 ICLK		
0008 A024h	SCI1	Serial Status Register	SSR	8	8	2 to 3PCLKB	2 ICLK		
0008 A025h	SCI1	Receive Data Register	RDR	8	8	2 to 3PCLKB	2 ICLK		
0008 A026h	SCI1	Smart Card Mode Register	SCMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A027h	SCI1	Serial Extended Mode Register	SEMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A028h	SCI1	Noise Filter Setting Register	SNFR	8	8	2 to 3PCLKB	2 ICLK		
0008 A029h	SCI1	I^2C Mode Register 1	SIMR1	8	8	2 to 3PCLKB	2 ICLK		
0008 A02Ah	SCI1	I^2C Mode Register 2	SIMR2	8	8	2 to 3PCLKB	2 ICLK		
0008 A02Bh	SCI1	I^2C Mode Register 3	SIMR3	8	8	2 to 3PCLKB	2 ICLK		
0008 A02Ch	SCI1	I^2C Status Register	SISR	8	8	2 to 3PCLKB	2 ICLK		
0008 A02Dh	SCI1	SPI Mode Register	SPMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A040h	SCI2	Serial Mode Register	SMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A041h	SCI2	Bit Rate Register	BRR	8	8	2 to 3PCLKB	2 ICLK		
0008 A042h	SCI2	Serial Control Register	SCR	8	8	2 to 3PCLKB	2 ICLK		
0008 A043h	SCI2	Transmit Data Register	TDR	8	8	2 to 3PCLKB	2 ICLK		
0008 A044h	SCI2	Serial Status Register	SSR	8	8	2 to 3PCLKB	2 ICLK		
0008 A045h	SCI2	Receive Data Register	RDR	8	8	2 to 3PCLKB	2 ICLK		
0008 A046h	SCI2	Smart Card Mode Register	SCMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A047h	SCI2	Serial Extended Mode Register	SEMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A048h	SCI2	Noise Filter Setting Register	SNFR	8	8	2 to 3PCLKB	2 ICLK		
0008 A049h	SCI2	I^2C Mode Register 1	SIMR1	8	8	2 to 3PCLKB	2 ICLK		
0008 A04Ah	SCI2	I^2C Mode Register 2	SIMR2	8	8	2 to 3PCLKB	2 ICLK		
0008 A04Bh	SCI2	I^2C Mode Register 3	SIMR3	8	8	2 to 3PCLKB	2 ICLK		
0008 A04Ch	SCI2	I^2C Status Register	SISR	8	8	2 to 3PCLKB	2 ICLK		
0008 A04Dh	SCI2	SPI Mode Register	SPMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A060h	SCI3	Serial Mode Register	SMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A061h	SCI3	Bit Rate Register	BRR	8	8	2 to 3PCLKB	2 ICLK		
0008 A062h	SCI3	Serial Control Register	SCR	8	8	2 to 3PCLKB	2 ICLK		
0008 A063h	SCI3	Transmit Data Register	TDR	8	8	2 to 3PCLKB	2 ICLK		
0008 A064h	SCI3	Serial Status Register	SSR	8	8	2 to 3PCLKB	2 ICLK		
0008 A065h	SCI3	Receive Data Register	RDR	8	8	2 to 3PCLKB	2 ICLK		
0008 A066h	SCI3	Smart Card Mode Register	SCMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A067h	SCI3	Serial Extended Mode Register	SEMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A068h	SCI3	Noise Filter Setting Register	SNFR	8	8	2 to 3PCLKB	2 ICLK		
0008 A069h	SCI3	I^2C Mode Register 1	SIMR1	8	8	2 to 3PCLKB	2 ICLK		
0008 A06Ah	SCI3	I^2C Mode Register 2	SIMR2	8	8	2 to 3PCLKB	2 ICLK		
0008 A06Bh	SCI3	I^2C Mode Register 3	SIMR3	8	8	2 to 3PCLKB	2 ICLK		
0008 A06Ch	SCI3	I^2C Status Register	SISR	8	8	2 to 3PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (22 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 A06Dh	SCI3	SPI Mode Register	SPMR	8	8	2 to 3PCLKB	2 ICLK	SCIe, SCIf	
0008 A080h	SCI4	Serial Mode Register	SMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A081h	SCI4	Bit Rate Register	BRR	8	8	2 to 3PCLKB	2 ICLK		
0008 A082h	SCI4	Serial Control Register	SCR	8	8	2 to 3PCLKB	2 ICLK		
0008 A083h	SCI4	Transmit Data Register	TDR	8	8	2 to 3PCLKB	2 ICLK		
0008 A084h	SCI4	Serial Status Register	SSR	8	8	2 to 3PCLKB	2 ICLK		
0008 A085h	SCI4	Receive Data Register	RDR	8	8	2 to 3PCLKB	2 ICLK		
0008 A086h	SCI4	Smart Card Mode Register	SCMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A087h	SCI4	Serial Extended Mode Register	SEMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A088h	SCI4	Noise Filter Setting Register	SNFR	8	8	2 to 3PCLKB	2 ICLK		
0008 A089h	SCI4	I^2C Mode Register 1	SIMR1	8	8	2 to 3PCLKB	2 ICLK		
0008 A08Ah	SCI4	I^2C Mode Register 2	SIMR2	8	8	2 to 3PCLKB	2 ICLK		
0008 A08Bh	SCI4	I^2C Mode Register 3	SIMR3	8	8	2 to 3PCLKB	2 ICLK		
0008 A08Ch	SCI4	I^2C Status Register	SISR	8	8	2 to 3PCLKB	2 ICLK		
0008 A08Dh	SCI4	SPI Mode Register	SPMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A0A0h	SCI5	Serial Mode Register	SMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A0A1h	SCI5	Bit Rate Register	BRR	8	8	2 to 3PCLKB	2 ICLK		
0008 A0A2h	SCI5	Serial Control Register	SCR	8	8	2 to 3PCLKB	2 ICLK		
0008 A0A3h	SCI5	Transmit Data Register	TDR	8	8	2 to 3PCLKB	2 ICLK		
0008 A0A4h	SCI5	Serial Status Register	SSR	8	8	2 to 3PCLKB	2 ICLK		
0008 A0A5h	SCI5	Receive Data Register	RDR	8	8	2 to 3PCLKB	2 ICLK		
0008 A0A6h	SCI5	Smart Card Mode Register	SCMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A0A7h	SCI5	Serial Extended Mode Register	SEMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A0A8h	SCI5	Noise Filter Setting Register	SNFR	8	8	2 to 3PCLKB	2 ICLK		
0008 A0A9h	SCI5	I^2C Mode Register 1	SIMR1	8	8	2 to 3PCLKB	2 ICLK		
0008 A0AAh	SCI5	I^2C Mode Register 2	SIMR2	8	8	2 to 3PCLKB	2 ICLK		
0008 A0ABh	SCI5	I^2C Mode Register 3	SIMR3	8	8	2 to 3PCLKB	2 ICLK		
0008 A0ACh	SCI5	I^2C Status Register	SISR	8	8	2 to 3PCLKB	2 ICLK		
0008 A0ADh	SCI5	SPI Mode Register	SPMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A0C0h	SCI6	Serial Mode Register	SMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A0C1h	SCI6	Bit Rate Register	BRR	8	8	2 to 3PCLKB	2 ICLK		
0008 A0C2h	SCI6	Serial Control Register	SCR	8	8	2 to 3PCLKB	2 ICLK		
0008 A0C3h	SCI6	Transmit Data Register	TDR	8	8	2 to 3PCLKB	2 ICLK		
0008 A0C4h	SCI6	Serial Status Register	SSR	8	8	2 to 3PCLKB	2 ICLK		
0008 A0C5h	SCI6	Receive Data Register	RDR	8	8	2 to 3PCLKB	2 ICLK		
0008 A0C6h	SCI6	Smart Card Mode Register	SCMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A0C7h	SCI6	Serial Extended Mode Register	SEMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A0C8h	SCI6	Noise Filter Setting Register	SNFR	8	8	2 to 3PCLKB	2 ICLK		
0008 A0C9h	SCI6	I^2C Mode Register 1	SIMR1	8	8	2 to 3PCLKB	2 ICLK		
0008 A0CAh	SCI6	I^2C Mode Register 2	SIMR2	8	8	2 to 3PCLKB	2 ICLK		
0008 A0CBh	SCI6	I^2C Mode Register 3	SIMR3	8	8	2 to 3PCLKB	2 ICLK		
0008 A0CCh	SCI6	I^2C Status Register	SISR	8	8	2 to 3PCLKB	2 ICLK		
0008 A0CDh	SCI6	SPI Mode Register	SPMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A0E0h	SCI7	Serial Mode Register	SMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A0E1h	SCI7	Bit Rate Register	BRR	8	8	2 to 3PCLKB	2 ICLK		
0008 A0E2h	SCI7	Serial Control Register	SCR	8	8	2 to 3PCLKB	2 ICLK		
0008 A0E3h	SCI7	Transmit Data Register	TDR	8	8	2 to 3PCLKB	2 ICLK		
0008 A0E4h	SCI7	Serial Status Register	SSR	8	8	2 to 3PCLKB	2 ICLK		
0008 A0E5h	SCI7	Receive Data Register	RDR	8	8	2 to 3PCLKB	2 ICLK		
0008 A0E6h	SCI7	Smart Card Mode Register	SCMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A0E7h	SCI7	Serial Extended Mode Register	SEMR	8	8	2 to 3PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (23 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 A0E8h	SCI7	Noise Filter Setting Register	SNFR	8	8	2 to 3PCLKB	2 ICLK	SCIe, SCIf	
0008 A0E9h	SCI7	I²C Mode Register 1	SIMR1	8	8	2 to 3PCLKB	2 ICLK		
0008 A0EAh	SCI7	I²C Mode Register 2	SIMR2	8	8	2 to 3PCLKB	2 ICLK		
0008 A0EBh	SCI7	I²C Mode Register 3	SIMR3	8	8	2 to 3PCLKB	2 ICLK		
0008 A0ECh	SCI7	I²C Status Register	SISR	8	8	2 to 3PCLKB	2 ICLK		
0008 A0EDh	SCI7	SPI Mode Register	SPMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A100h	SCI8	Serial Mode Register	SMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A101h	SCI8	Bit Rate Register	BRR	8	8	2 to 3PCLKB	2 ICLK		
0008 A102h	SCI8	Serial Control Register	SCR	8	8	2 to 3PCLKB	2 ICLK		
0008 A103h	SCI8	Transmit Data Register	TDR	8	8	2 to 3PCLKB	2 ICLK		
0008 A104h	SCI8	Serial Status Register	SSR	8	8	2 to 3PCLKB	2 ICLK		
0008 A105h	SCI8	Receive Data Register	RDR	8	8	2 to 3PCLKB	2 ICLK		
0008 A106h	SCI8	Smart Card Mode Register	SCMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A107h	SCI8	Serial Extended Mode Register	SEMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A108h	SCI8	Noise Filter Setting Register	SNFR	8	8	2 to 3PCLKB	2 ICLK		
0008 A109h	SCI8	I²C Mode Register 1	SIMR1	8	8	2 to 3PCLKB	2 ICLK		
0008 A10Ah	SCI8	I²C Mode Register 2	SIMR2	8	8	2 to 3PCLKB	2 ICLK		
0008 A10Bh	SCI8	I²C Mode Register 3	SIMR3	8	8	2 to 3PCLKB	2 ICLK		
0008 A10Ch	SCI8	I²C Status Register	SISR	8	8	2 to 3PCLKB	2 ICLK		
0008 A10Dh	SCI8	SPI Mode Register	SPMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A120h	SCI9	Serial Mode Register	SMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A121h	SCI9	Bit Rate Register	BRR	8	8	2 to 3PCLKB	2 ICLK		
0008 A122h	SCI9	Serial Control Register	SCR	8	8	2 to 3PCLKB	2 ICLK		
0008 A123h	SCI9	Transmit Data Register	TDR	8	8	2 to 3PCLKB	2 ICLK		
0008 A124h	SCI9	Serial Status Register	SSR	8	8	2 to 3PCLKB	2 ICLK		
0008 A125h	SCI9	Receive Data Register	RDR	8	8	2 to 3PCLKB	2 ICLK		
0008 A126h	SCI9	Smart Card Mode Register	SCMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A127h	SCI9	Serial Extended Mode Register	SEMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A128h	SCI9	Noise Filter Setting Register	SNFR	8	8	2 to 3PCLKB	2 ICLK		
0008 A129h	SCI9	I²C Mode Register 1	SIMR1	8	8	2 to 3PCLKB	2 ICLK		
0008 A12Ah	SCI9	I²C Mode Register 2	SIMR2	8	8	2 to 3PCLKB	2 ICLK		
0008 A12Bh	SCI9	I²C Mode Register 3	SIMR3	8	8	2 to 3PCLKB	2 ICLK		
0008 A12Ch	SCI9	I²C Status Register	SISR	8	8	2 to 3PCLKB	2 ICLK		
0008 A12Dh	SCI9	SPI Mode Register	SPMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A140h	SCI10	Serial Mode Register	SMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A141h	SCI10	Bit Rate Register	BRR	8	8	2 to 3PCLKB	2 ICLK		
0008 A142h	SCI10	Serial Control Register	SCR	8	8	2 to 3PCLKB	2 ICLK		
0008 A143h	SCI10	Transmit Data Register	TDR	8	8	2 to 3PCLKB	2 ICLK		
0008 A144h	SCI10	Serial Status Register	SSR	8	8	2 to 3PCLKB	2 ICLK		
0008 A145h	SCI10	Receive Data Register	RDR	8	8	2 to 3PCLKB	2 ICLK		
0008 A146h	SCI10	Smart Card Mode Register	SCMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A147h	SCI10	Serial Extended Mode Register	SEMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A148h	SCI10	Noise Filter Setting Register	SNFR	8	8	2 to 3PCLKB	2 ICLK		
0008 A149h	SCI10	I²C Mode Register 1	SIMR1	8	8	2 to 3PCLKB	2 ICLK		
0008 A14Ah	SCI10	I²C Mode Register 2	SIMR2	8	8	2 to 3PCLKB	2 ICLK		
0008 A14Bh	SCI10	I²C Mode Register 3	SIMR3	8	8	2 to 3PCLKB	2 ICLK		
0008 A14Ch	SCI10	I²C Status Register	SISR	8	8	2 to 3PCLKB	2 ICLK		
0008 A14Dh	SCI10	SPI Mode Register	SPMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A160h	SCI11	Serial Mode Register	SMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A161h	SCI11	Bit Rate Register	BRR	8	8	2 to 3PCLKB	2 ICLK		
0008 A162h	SCI11	Serial Control Register	SCR	8	8	2 to 3PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (24 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 A163h	SCI11	Transmit Data Register	TDR	8	8	2 to 3PCLKB	2 ICLK	SCIe, SCIf	
0008 A164h	SCI11	Serial Status Register	SSR	8	8	2 to 3PCLKB	2 ICLK		
0008 A165h	SCI11	Receive Data Register	RDR	8	8	2 to 3PCLKB	2 ICLK		
0008 A166h	SCI11	Smart Card Mode Register	SCMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A167h	SCI11	Serial Extended Mode Register	SEMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A168h	SCI11	Noise Filter Setting Register	SNFR	8	8	2 to 3PCLKB	2 ICLK		
0008 A169h	SCI11	I^2C Mode Register 1	SIMR1	8	8	2 to 3PCLKB	2 ICLK		
0008 A16Ah	SCI11	I^2C Mode Register 2	SIMR2	8	8	2 to 3PCLKB	2 ICLK		
0008 A16Bh	SCI11	I^2C Mode Register 3	SIMR3	8	8	2 to 3PCLKB	2 ICLK		
0008 A16Ch	SCI11	I^2C Status Register	SISR	8	8	2 to 3PCLKB	2 ICLK		
0008 A16Dh	SCI11	SPI Mode Register	SPMR	8	8	2 to 3PCLKB	2 ICLK		
0008 B000h	CAC	CAC Control Register 0	CACR0	8	8	2 to 3PCLKB	2 ICLK	CAC	
0008 B001h	CAC	CAC Control Register 1	CACR1	8	8	2 to 3PCLKB	2 ICLK		
0008 B002h	CAC	CAC Control Register 2	CACR2	8	8	2 to 3PCLKB	2 ICLK		
0008 B003h	CAC	CAC Interrupt Request Enable Register	CAICR	8	8	2 to 3PCLKB	2 ICLK		
0008 B004h	CAC	CAC Status Register	CASTR	8	8	2 to 3PCLKB	2 ICLK		
0008 B006h	CAC	CAC Upper-Limit Value Setting Register	CAULVR	16	16	2 to 3PCLKB	2 ICLK		
0008 B008h	CAC	CAC Lower-Limit Value Setting Register	CALLVR	16	16	2 to 3PCLKB	2 ICLK		
0008 B00Ah	CAC	CAC Counter Buffer Register	CACNTBR	16	16	2 to 3PCLKB	2 ICLK		
0008 B080h	DOC	DOC Control Register	DOCR	8	8	2 to 3PCLKB	2 ICLK	DOC	
0008 B082h	DOC	DOC Data Input Register	DODIR	16	16	2 to 3PCLKB	2 ICLK		
0008 B084h	DOC	DOC Data Setting Register	DODSR	16	16	2 to 3PCLKB	2 ICLK		
0008 B100h	ELC	Event Link Control Register	ELCR	8	8	2 to 3PCLKB	2 ICLK	ELC	
0008 B102h	ELC	Event Link Setting Register 1	ELSR1	8	8	2 to 3PCLKB	2 ICLK		
0008 B103h	ELC	Event Link Setting Register 2	ELSR2	8	8	2 to 3PCLKB	2 ICLK		
0008 B104h	ELC	Event Link Setting Register 3	ELSR3	8	8	2 to 3PCLKB	2 ICLK		
0008 B105h	ELC	Event Link Setting Register 4	ELSR4	8	8	2 to 3PCLKB	2 ICLK		
0008 B108h	ELC	Event Link Setting Register 7	ELSR7	8	8	2 to 3PCLKB	2 ICLK		
0008 B10Bh	ELC	Event Link Setting Register 10	ELSR10	8	8	2 to 3PCLKB	2 ICLK		
0008 B10Dh	ELC	Event Link Setting Register 12	ELSR12	8	8	2 to 3PCLKB	2 ICLK		
0008 B110h	ELC	Event Link Setting Register 15	ELSR15	8	8	2 to 3PCLKB	2 ICLK		
0008 B111h	ELC	Event Link Setting Register 16	ELSR16	8	8	2 to 3PCLKB	2 ICLK		
0008 B113h	ELC	Event Link Setting Register 18	ELSR18	8	8	2 to 3PCLKB	2 ICLK		
0008 B114h	ELC	Event Link Setting Register 19	ELSR19	8	8	2 to 3PCLKB	2 ICLK		
0008 B115h	ELC	Event Link Setting Register 20	ELSR20	8	8	2 to 3PCLKB	2 ICLK		
0008 B116h	ELC	Event Link Setting Register 21	ELSR21	8	8	2 to 3PCLKB	2 ICLK		
0008 B117h	ELC	Event Link Setting Register 22	ELSR22	8	8	2 to 3PCLKB	2 ICLK		
0008 B118h	ELC	Event Link Setting Register 23	ELSR23	8	8	2 to 3PCLKB	2 ICLK		
0008 B119h	ELC	Event Link Setting Register 24	ELSR24	8	8	2 to 3PCLKB	2 ICLK		
0008 B11Ah	ELC	Event Link Setting Register 25	ELSR25	8	8	2 to 3PCLKB	2 ICLK		
0008 B11Bh	ELC	Event Link Setting Register 26	ELSR26	8	8	2 to 3PCLKB	2 ICLK		
0008 B11Ch	ELC	Event Link Setting Register 27	ELSR27	8	8	2 to 3PCLKB	2 ICLK		
0008 B11Dh	ELC	Event Link Setting Register 28	ELSR28	8	8	2 to 3PCLKB	2 ICLK		
0008 B11Eh	ELC	Event Link Setting Register 29	ELSR29	8	8	2 to 3PCLKB	2 ICLK		
0008 B11Fh	ELC	Event Link Option Setting Register A	ELOPA	8	8	2 to 3PCLKB	2 ICLK		
0008 B120h	ELC	Event Link Option Setting Register B	ELOPB	8	8	2 to 3PCLKB	2 ICLK		
0008 B121h	ELC	Event Link Option Setting Register C	ELOPC	8	8	2 to 3PCLKB	2 ICLK		
0008 B122h	ELC	Event Link Option Setting Register D	ELOPD	8	8	2 to 3PCLKB	2 ICLK		
0008 B123h	ELC	Port Group Setting Register 1	PGR1	8	8	2 to 3PCLKB	2 ICLK		
0008 B124h	ELC	Port Group Setting Register 2	PGR2	8	8	2 to 3PCLKB	2 ICLK		
0008 B125h	ELC	Port Group Control Register 1	PGC1	8	8	2 to 3PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (25 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 B126h	ELC	Port Group Control Register 2	PGC2	8	8	2 to 3PCLKB	2 ICLK	ELC	
0008 B127h	ELC	Port Buffer Register 1	PDBF1	8	8	2 to 3PCLKB	2 ICLK		
0008 B128h	ELC	Port Buffer Register 2	PDBF2	8	8	2 to 3PCLKB	2 ICLK		
0008 B129h	ELC	Event Link Port Setting Register 0	PEL0	8	8	2 to 3PCLKB	2 ICLK		
0008 B12Ah	ELC	Event Link Port Setting Register 1	PEL1	8	8	2 to 3PCLKB	2 ICLK		
0008 B12Bh	ELC	Event Link Port Setting Register 2	PEL2	8	8	2 to 3PCLKB	2 ICLK		
0008 B12Ch	ELC	Event Link Port Setting Register 3	PEL3	8	8	2 to 3PCLKB	2 ICLK		
0008 B12Dh	ELC	Event Link Software Event Generation Register	ELSEGR	8	8	2 to 3PCLKB	2 ICLK		
0008 B300h	SCI12	Serial Mode Register	SMR	8	8	2 to 3PCLKB	2 ICLK	SCIe, SCIf	
0008 B301h	SCI12	Bit Rate Register	BRR	8	8	2 to 3PCLKB	2 ICLK		
0008 B302h	SCI12	Serial Control Register	SCR	8	8	2 to 3PCLKB	2 ICLK		
0008 B303h	SCI12	Transmit Data Register	TDR	8	8	2 to 3PCLKB	2 ICLK		
0008 B304h	SCI12	Serial Status Register	SSR	8	8	2 to 3PCLKB	2 ICLK		
0008 B305h	SCI12	Receive Data Register	RDR	8	8	2 to 3PCLKB	2 ICLK		
0008 B306h	SCI12	Smart Card Mode Register	SCMR	8	8	2 to 3PCLKB	2 ICLK		
0008 B307h	SCI12	Serial Extended Mode Register	SEMR	8	8	2 to 3PCLKB	2 ICLK		
0008 B308h	SCI12	Noise Filter Setting Register	SNFR	8	8	2 to 3PCLKB	2 ICLK		
0008 B309h	SCI12	I^2C Mode Register 1	SIMR1	8	8	2 to 3PCLKB	2 ICLK		
0008 B30Ah	SCI12	I^2C Mode Register 2	SIMR2	8	8	2 to 3PCLKB	2 ICLK		
0008 B30Bh	SCI12	I^2C Mode Register 3	SIMR3	8	8	2 to 3PCLKB	2 ICLK		
0008 B30Ch	SCI12	I^2C Status Register	SISR	8	8	2 to 3PCLKB	2 ICLK		
0008 B30Dh	SCI12	SPI Mode Register	SPMR	8	8	2 to 3PCLKB	2 ICLK		
0008 B320h	SCI12	Extended Serial Module Enable Register	ESMER	8	8	2 to 3PCLKB	2 ICLK		
0008 B321h	SCI12	Control Register 0	CR0	8	8	2 to 3PCLKB	2 ICLK		
0008 B322h	SCI12	Control Register 1	CR1	8	8	2 to 3PCLKB	2 ICLK		
0008 B323h	SCI12	Control Register 2	CR2	8	8	2 to 3PCLKB	2 ICLK		
0008 B324h	SCI12	Control Register 3	CR3	8	8	2 to 3PCLKB	2 ICLK		
0008 B325h	SCI12	Port Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 B326h	SCI12	Interrupt Control Register	ICR	8	8	2 to 3PCLKB	2 ICLK		
0008 B327h	SCI12	Status Register	STR	8	8	2 to 3PCLKB	2 ICLK		
0008 B328h	SCI12	Status Clear Register	STCR	8	8	2 to 3PCLKB	2 ICLK		
0008 B329h	SCI12	Control Field 0 Data Register	CF0DR	8	8	2 to 3PCLKB	2 ICLK		
0008 B32Ah	SCI12	Control Field 0 Compare Enable Register	CF0CR	8	8	2 to 3PCLKB	2 ICLK		
0008 B32Bh	SCI12	Control Field 0 Receive Data Register	CF0RR	8	8	2 to 3PCLKB	2 ICLK		
0008 B32Ch	SCI12	Primary Control Field 1 Data Register	PCF1DR	8	8	2 to 3PCLKB	2 ICLK		
0008 B32Dh	SCI12	Secondary Control Field 1 Data Register	SCF1DR	8	8	2 to 3PCLKB	2 ICLK		
0008 B32Eh	SCI12	Control Field 1 Compare Enable Register	CF1CR	8	8	2 to 3PCLKB	2 ICLK		
0008 B32Fh	SCI12	Control Field 1 Receive Data Register	CF1RR	8	8	2 to 3PCLKB	2 ICLK		
0008 B330h	SCI12	Timer Control Register	TCR	8	8	2 to 3PCLKB	2 ICLK		
0008 B331h	SCI12	Timer Mode Register	TMR	8	8	2 to 3PCLKB	2 ICLK		
0008 B332h	SCI12	Timer Prescaler Register	TPRE	8	8	2 to 3PCLKB	2 ICLK		
0008 B333h	SCI12	Timer Count Register	TCNT	8	8	2 to 3PCLKB	2 ICLK		
0008 C000h	PORT0	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK	I/O Ports	
0008 C001h	PORT1	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C002h	PORT2	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C003h	PORT3	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C005h	PORT5	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C006h	PORT6	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C007h	PORT7	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C008h	PORT8	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C009h	PORT9	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (26 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 C00Ah	PORTA	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK	I/O Ports	
0008 C00Bh	PORTB	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C00Ch	PORTC	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C00Dh	PORTD	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C00Eh	PORTE	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C00Fh	PORTF	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C011h	PORTH	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C012h	PORTJ	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C013h	PORTK	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C014h	PORTL	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C020h	PORT0	Port Output Data Register	PODR	8	8	2 to 3PCLKB	2 ICLK		
0008 C021h	PORT1	Port Output Data Register	PODR	8	8	2 to 3PCLKB	2 ICLK		
0008 C022h	PORT2	Port Output Data Register	PODR	8	8	2 to 3PCLKB	2 ICLK		
0008 C023h	PORT3	Port Output Data Register	PODR	8	8	2 to 3PCLKB	2 ICLK		
0008 C025h	PORT5	Port Output Data Register	PODR	8	8	2 to 3PCLKB	2 ICLK		
0008 C026h	PORT6	Port Output Data Register	PODR	8	8	2 to 3PCLKB	2 ICLK		
0008 C027h	PORT7	Port Output Data Register	PODR	8	8	2 to 3PCLKB	2 ICLK		
0008 C028h	PORT8	Port Output Data Register	PODR	8	8	2 to 3PCLKB	2 ICLK		
0008 C029h	PORT9	Port Output Data Register	PODR	8	8	2 to 3PCLKB	2 ICLK		
0008 C02Ah	PORTA	Port Output Data Register	PODR	8	8	2 to 3PCLKB	2 ICLK		
0008 C02Bh	PORTB	Port Output Data Register	PODR	8	8	2 to 3PCLKB	2 ICLK		
0008 C02Ch	PORTC	Port Output Data Register	PODR	8	8	2 to 3PCLKB	2 ICLK		
0008 C02Dh	PORTD	Port Output Data Register	PODR	8	8	2 to 3PCLKB	2 ICLK		
0008 C02Eh	PORTE	Port Output Data Register	PODR	8	8	2 to 3PCLKB	2 ICLK		
0008 C02Fh	PORTF	Port Output Data Register	PODR	8	8	2 to 3PCLKB	2 ICLK		
0008 C031h	PORTH	Port Output Data Register	PODR	8	8	2 to 3PCLKB	2 ICLK		
0008 C032h	PORTJ	Port Output Data Register	PODR	8	8	2 to 3PCLKB	2 ICLK		
0008 C033h	PORTK	Port Output Data Register	PODR	8	8	2 to 3PCLKB	2 ICLK		
0008 C034h	PORTL	Port Output Data Register	PODR	8	8	2 to 3PCLKB	2 ICLK		
0008 C040h	PORT0	Port Input Data Register	PIDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C041h	PORT1	Port Input Data Register	PIDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C042h	PORT2	Port Input Data Register	PIDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C043h	PORT3	Port Input Data Register	PIDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C044h	PORT4	Port Input Data Register	PIDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C045h	PORT5	Port Input Data Register	PIDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C046h	PORT6	Port Input Data Register	PIDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C047h	PORT7	Port Input Data Register	PIDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C048h	PORT8	Port Input Data Register	PIDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C049h	PORT9	Port Input Data Register	PIDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C04Ah	PORTA	Port Input Data Register	PIDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C04Bh	PORTB	Port Input Data Register	PIDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C04Ch	PORTC	Port Input Data Register	PIDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C04Dh	PORTD	Port Input Data Register	PIDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C04Eh	PORTE	Port Input Data Register	PIDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C04Fh	PORTF	Port Input Data Register	PIDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C051h	PORTH	Port Input Data Register	PIDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C052h	PORTJ	Port Input Data Register	PIDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C053h	PORTK	Port Input Data Register	PIDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C054h	PORTL	Port Input Data Register	PIDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C060h	PORT0	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C061h	PORT1	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (27 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 C062h	PORT2	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK	I/O Ports	
0008 C063h	PORT3	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C065h	PORT5	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C066h	PORT6	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C067h	PORT7	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C068h	PORT8	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C069h	PORT9	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C06Ah	PORTA	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C06Bh	PORTB	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C06Ch	PORTC	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C06Dh	PORTD	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C06Eh	PORTE	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C06Fh	PORTF	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C071h	PORTH	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C072h	PORTJ	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C073h	PORTK	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C074h	PORTL	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C080h	PORT0	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C082h	PORT1	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C083h	PORT1	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C084h	PORT2	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C085h	PORT2	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C086h	PORT3	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C087h	PORT3	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C08Ah	PORT5	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C08Bh	PORT5	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C08Ch	PORT6	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C08Eh	PORT7	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C08Fh	PORT7	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C090h	PORT8	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C092h	PORT9	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C094h	PORTA	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C095h	PORTA	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C096h	PORTB	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C097h	PORTB	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C098h	PORTC	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C099h	PORTC	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C09Ch	PORTE	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C09Dh	PORTE	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C0A6h	PORTK	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C0A7h	PORTK	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C0C0h	PORT0	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0C1h	PORT1	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0C2h	PORT2	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0C3h	PORT3	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0C5h	PORT5	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0C6h	PORT6	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0C7h	PORT7	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0C8h	PORT8	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0C9h	PORT9	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0CAh	PORTA	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (28 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 C0CBh	PORTB	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK	I/O Ports	
0008 C0CCh	PORTC	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0CDh	PORTD	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0CEh	PORTE	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0CFh	PORTF	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0D1h	PORTH	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0D2h	PORTJ	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0D3h	PORTK	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0D4h	PORTL	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0E0h	PORT0	Drive Capacity Control Register	DSCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0E1h	PORT1	Drive Capacity Control Register	DSCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0E2h	PORT2	Drive Capacity Control Register	DSCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0E3h	PORT3	Drive Capacity Control Register	DSCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0E5h	PORT5	Drive Capacity Control Register	DSCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0E6h	PORT6	Drive Capacity Control Register	DSCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0E7h	PORT7	Drive Capacity Control Register	DSCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0E8h	PORT8	Drive Capacity Control Register	DSCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0E9h	PORT9	Drive Capacity Control Register	DSCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0EAh	PORTA	Drive Capacity Control Register	DSCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0EBh	PORTB	Drive Capacity Control Register	DSCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0ECh	PORTC	Drive Capacity Control Register	DSCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0EDh	PORTD	Drive Capacity Control Register	DSCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0EEh	PORTE	Drive Capacity Control Register	DSCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0F1h	PORTH	Drive Capacity Control Register	DSCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0F2h	PORTJ	Drive Capacity Control Register	DSCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0F3h	PORTK	Drive Capacity Control Register	DSCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C100h	MPC	CS Output Enable Register	PFCSE	8	8	2 to 3PCLKB	2 ICLK	MPC	
0008 C104h	MPC	Address Output Enable Register 0	PFAOE0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C105h	MPC	Address Output Enable Register 1	PFAOE1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C106h	MPC	External Bus Control Register 0	PFBCR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C107h	MPC	External Bus Control Register 1	PFBCR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C11Fh	MPC	Write-Protect Register	PWPR	8	8	2 to 3PCLKB	2 ICLK		
0008 C140h	MPC	P00 Pin Function Control Register	P00PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C141h	MPC	P01 Pin Function Control Register	P01PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C142h	MPC	P02 Pin Function Control Register	P02PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C143h	MPC	P03 Pin Function Control Register	P03PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C145h	MPC	P05 Pin Function Control Register	P05PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C147h	MPC	P07 Pin Function Control Register	P07PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C14Ah	MPC	P12 Pin Function Control Registers	P12PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C14Bh	MPC	P13 Pin Function Control Registers	P13PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C14Ch	MPC	P14 Pin Function Control Registers	P14PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C14Dh	MPC	P15 Pin Function Control Registers	P15PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C14Eh	MPC	P16 Pin Function Control Registers	P16PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C14Fh	MPC	P17 Pin Function Control Registers	P17PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C150h	MPC	P20 Pin Function Control Register	P20PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C151h	MPC	P21 Pin Function Control Register	P21PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C152h	MPC	P22 Pin Function Control Register	P22PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C153h	MPC	P23 Pin Function Control Register	P23PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C154h	MPC	P24 Pin Function Control Register	P24PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C155h	MPC	P25 Pin Function Control Register	P25PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C156h	MPC	P26 Pin Function Control Register	P26PFS	8	8	2 to 3PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (29 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 C157h	MPC	P27 Pin Function Control Register	P27PFS	8	8	2 to 3PCLKB	2 ICLK	MPC	
0008 C158h	MPC	P30 Pin Function Control Registers	P30PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C159h	MPC	P31 Pin Function Control Registers	P31PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C15Ah	MPC	P32 Pin Function Control Registers	P32PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C15Bh	MPC	P33 Pin Function Control Registers	P33PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C15Ch	MPC	P34 Pin Function Control Registers	P34PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C160h	MPC	P40 Pin Function Control Registers	P40PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C161h	MPC	P41 Pin Function Control Registers	P41PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C162h	MPC	P42 Pin Function Control Registers	P42PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C163h	MPC	P43 Pin Function Control Registers	P43PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C164h	MPC	P44 Pin Function Control Registers	P44PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C165h	MPC	P45 Pin Function Control Registers	P45PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C166h	MPC	P46 Pin Function Control Registers	P46PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C167h	MPC	P47 Pin Function Control Registers	P47PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C168h	MPC	P50 Pin Function Control Registers	P50PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C169h	MPC	P51 Pin Function Control Registers	P51PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C16Ah	MPC	P52 Pin Function Control Registers	P52PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C16Ch	MPC	P54 Pin Function Control Registers	P54PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C16Dh	MPC	P55 Pin Function Control Registers	P55PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C16Eh	MPC	P56 Pin Function Control Registers	P56PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C170h	MPC	P60 Pin Function Control Registers	P60PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C171h	MPC	P61 Pin Function Control Registers	P61PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C178h	MPC	P70 Pin Function Control Registers	P70PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C17Bh	MPC	P73 Pin Function Control Registers	P73PFS	8	8	2 to 3PCLKB	2 ICLK		Not available in 3-V packages.
0008 C17Ch	MPC	P74 Pin Function Control Registers	P74PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C17Dh	MPC	P75 Pin Function Control Registers	P75PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C17Eh	MPC	P76 Pin Function Control Registers	P76PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C17Fh	MPC	P77 Pin Function Control Registers	P77PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C180h	MPC	P80 Pin Function Control Registers	P80PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C181h	MPC	P81 Pin Function Control Registers	P81PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C182h	MPC	P82 Pin Function Control Registers	P82PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C183h	MPC	P83 Pin Function Control Registers	P83PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C186h	MPC	P86 Pin Function Control Registers	P86PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C187h	MPC	P87 Pin Function Control Registers	P87PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C188h	MPC	P90 Pin Function Control Registers	P90PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C189h	MPC	P91 Pin Function Control Registers	P91PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C18Ah	MPC	P92 Pin Function Control Registers	P92PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C18Bh	MPC	P93 Pin Function Control Registers	P93PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C190h	MPC	PA0 Pin Function Control Registers	PA0PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C191h	MPC	PA1 Pin Function Control Registers	PA1PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C192h	MPC	PA2 Pin Function Control Registers	PA2PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C193h	MPC	PA3 Pin Function Control Registers	PA3PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C194h	MPC	PA4 Pin Function Control Registers	PA4PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C195h	MPC	PA5 Pin Function Control Registers	PA5PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C196h	MPC	PA6 Pin Function Control Registers	PA6PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C197h	MPC	PA7 Pin Function Control Registers	PA7PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C198h	MPC	PB0 Pin Function Control Registers	PB0PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C199h	MPC	PB1 Pin Function Control Registers	PB1PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C19Ah	MPC	PB2 Pin Function Control Registers	PB2PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C19Bh	MPC	PB3 Pin Function Control Registers	PB3PFS	8	8	2 to 3PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (30 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 C19Ch	MPC	PB4 Pin Function Control Registers	PB4PFS	8	8	2 to 3PCLKB	2 ICLK	MPC	
0008 C19Dh	MPC	PB5 Pin Function Control Registers	PB5PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C19Eh	MPC	PB6 Pin Function Control Registers	PB6PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C19Fh	MPC	PB7 Pin Function Control Registers	PB7PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1A0h	MPC	PC0 Pin Function Control Registers	PC0PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1A1h	MPC	PC1 Pin Function Control Registers	PC1PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1A2h	MPC	PC2 Pin Function Control Registers	PC2PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1A3h	MPC	PC3 Pin Function Control Registers	PC3PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1A4h	MPC	PC4 Pin Function Control Registers	PC4PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1A5h	MPC	PC5 Pin Function Control Registers	PC5PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1A6h	MPC	PC6 Pin Function Control Registers	PC6PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1A7h	MPC	PC7 Pin Function Control Registers	PC7PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1A8h	MPC	PD0 Pin Function Control Registers	PD0PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1A9h	MPC	PD1 Pin Function Control Registers	PD1PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1AAh	MPC	PD2 Pin Function Control Registers	PD2PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1ABh	MPC	PD3 Pin Function Control Registers	PD3PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1ACh	MPC	PD4 Pin Function Control Registers	PD4PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1ADh	MPC	PD5 Pin Function Control Registers	PD5PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1AEh	MPC	PD6 Pin Function Control Registers	PD6PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1AFh	MPC	PD7 Pin Function Control Registers	PD7PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1B0h	MPC	PE0 Pin Function Control Registers	PE0PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1B1h	MPC	PE1 Pin Function Control Registers	PE1PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1B2h	MPC	PE2 Pin Function Control Registers	PE2PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1B3h	MPC	PE3 Pin Function Control Registers	PE3PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1B4h	MPC	PE4 Pin Function Control Registers	PE4PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1B5h	MPC	PE5 Pin Function Control Registers	PE5PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1B6h	MPC	PE6 Pin Function Control Registers	PE6PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1B7h	MPC	PE7 Pin Function Control Registers	PE7PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1BDh	MPC	PF5 Pin Function Control Registers	PF5PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1C8h	MPC	PH0 Pin Function Control Registers	PH0PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1C9h	MPC	PH1 Pin Function Control Registers	PH1PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1CAh	MPC	PH2 Pin Function Control Registers	PH2PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1CBh	MPC	PH3 Pin Function Control Registers	PH3PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1D1h	MPC	PJ1 Pin Function Control Registers	PJ1PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1D3h	MPC	PJ3 Pin Function Control Registers	PJ3PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1DAh	MPC	PK2 Pin Function Control Registers	PK2PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1DBh	MPC	PK3 Pin Function Control Registers	PK3PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1DCh	MPC	PK4 Pin Function Control Registers	PK4PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1DDh	MPC	PK5 Pin Function Control Registers	PK5PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1E5h	MPC	PL5 Pin Function Control Register	PL5PFS	8	8	2 to 3PCLKB	2 ICLK		Not available in 5-V packages.
0008 C280h	SYSTEM	Deep Standby Control Register	DPSBYCR	8	8	4 to 5PCLKB	2 to 3 ICLK	Low Power Consumption	
0008 C282h	SYSTEM	Deep Standby Interrupt Enable Register 0	DPSIER0	8	8	4 to 5PCLKB	2 to 3 ICLK		
0008 C284h	SYSTEM	Deep Standby Interrupt Enable Register 2	DPSIER2	8	8	4 to 5PCLKB	2 to 3 ICLK		
0008 C286h	SYSTEM	Deep Standby Interrupt Flag Register 0	DPSIFR0	8	8	4 to 5PCLKB	2 to 3 ICLK		
0008 C288h	SYSTEM	Deep Standby Interrupt Flag Register 2	DPSIFR2	8	8	4 to 5PCLKB	2 to 3 ICLK		
0008 C28Ah	SYSTEM	Deep Standby Interrupt Edge Register 0	DPSIEGR0	8	8	4 to 5PCLKB	2 to 3 ICLK		
0008 C28Ch	SYSTEM	Deep Standby Interrupt Edge Register 2	DPSIEGR2	8	8	4 to 5PCLKB	2 to 3 ICLK		
0008 C290h	SYSTEM	Reset Status Register 0	RSTSR0	8	8	4 to 5PCLKB	2 to 3 ICLK	Resets	
0008 C291h	SYSTEM	Reset Status Register 1	RSTSR1	8	8	4 to 5PCLKB	2 to 3 ICLK		

Table 4.1 List of I/O Registers (Address Order) (31 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 C293h	SYSTEM	Main Clock Oscillator Forced Oscillation Control Register	MOFCR	8	8	4 to 5PCLKB	2 to 3 ICLK	Clock Generation Circuit	
0008 C296h	FLASH	Flash Write Erase Protection Register	FWEPROR	8	8	4 to 5PCLKB	2 to 3 ICLK	Flash Memory	
0008 C297h	SYSTEM	Voltage Monitoring Circuit Control Register	LVCMPCR	8	8	4 to 5PCLKB	2 to 3 ICLK	LVDA	
0008 C298h	SYSTEM	Voltage Detection Level Select Register	LVDLVLR	8	8	4 to 5PCLKB	2 to 3 ICLK		
0008 C29Ah	SYSTEM	Voltage Monitoring 1 Circuit Control Register 0	LVD1CR0	8	8	4 to 5PCLKB	2 to 3 ICLK		
0008 C29Bh	SYSTEM	Voltage Monitoring 2 Circuit Control Register 0	LVD2CR0	8	8	4 to 5PCLKB	2 to 3 ICLK		
0008 C2A0h to 0008 C2BFh	SYSTEM	Deep Standby Backup Register 0 to 31	DPSBKR0 to 31	8	8	4 to 5PCLKB	2 to 3 ICLK	Low Power Consumption	
000A 0A00h	CEC	CEC Local Address Setting Register	CADR	16	16	1 to 2PCLK	1 ICLK	CEC	Not available in 5-V packages.
000A 0A02h	CEC	CEC Control Register 1	CECCTL1	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A04h	CEC	CEC Transmission Start Bit Width Setting Register	STATB	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A06h	CEC	CEC Transmission Start Bit Low Width Setting Register	STATL	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A08h	CEC	CEC Transmission Logical 0 Low Width Setting Register	LGC0L	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A0Ah	CEC	CEC Transmission Logical 1 Low Width Setting Register	LGC1L	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A0Ch	CEC	CEC Transmission Data Bit Width Setting Register	DATB	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A0Eh	CEC	CEC Reception Data Sampling Time Setting Register	NOMT	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A10h	CEC	CEC Reception Start Bit Minimum Low Width Setting Register	STATLL	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A12h	CEC	CEC Reception Start Bit Maximum Low Width Setting Register	STATLH	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A14h	CEC	CEC Reception Start Bit Minimum Bit Width Setting Register	STATBL	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A16h	CEC	CEC Reception Start Bit Maximum Bit Width Setting Register	STATBH	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A18h	CEC	CEC Reception Logical 0 Minimum Low Width Setting Register	LGC0LL	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A1Ah	CEC	CEC Reception Logical 0 Maximum Low Width Setting Register	LGC0LH	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A1Ch	CEC	CEC Reception Logical 1 Minimum Low Width Setting Register	LGC1LL	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A1Eh	CEC	CEC Reception Logical 1 Maximum Low Width Setting Register	LGC1LH	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A20h	CEC	CEC Reception Data Bit Minimum Bit Width Setting Register	DATBL	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A22h	CEC	CEC Reception Data Bit Maximum Bit Width Setting Register	DATBH	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A24h	CEC	CEC Data Bit Reference Width Setting Register	NOMP	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.

Table 4.1 List of I/O Registers (Address Order) (32 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000A 0A28h	CEC	CEC Extension Mode Register	CECEXMD	8	8	1 to 2PCLK	1 ICLK	CEC	Not available in 5-V packages.
000A 0A2Ah	CEC	CEC Extension Monitor Register	CECEXMON	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A30h	CEC	CEC Transmission Buffer Register	CTXD	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A31h	CEC	CEC Reception Buffer Register	CRXD	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A32h	CEC	CEC Communication Error Status Register	CECES	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A33h	CEC	CEC Communication Status Register	CECS	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A34h	CEC	CEC Communication Error Flag Clear Trigger Register	CECFC	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A35h	CEC	CEC Control Register 0	CECCTL0	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B00h	RCR0	Function Select Register 0	CON0	8	8	1 to 2PCLK	1 ICLK	RCR	Not available in 5-V packages.
000A 0B01h	RCR0	Function Select Register 1	CON1	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B02h	RCR0	Status Register	STS	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B03h	RCR0	Interrupt Control Register	INT	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B04h	RCR0	Compare Control Register	CPC	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B05h	RCR0	Compare Value Setting Register	CPD	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B06h	RCR0	Header Pattern Setting Register (Min)	HDPMIN	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B08h	RCR0	Header Pattern Setting Register (Max)	HDPMAX	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B0Ah	RCR0	Data 0 Pattern Setting Register (Min)	D0PMIN	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B0Bh	RCR0	Data 0 Pattern Setting Register (Max)	D0PMAX	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B0Ch	RCR0	Data 1 Pattern Setting Register (Min)	D1PMIN	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B0Dh	RCR0	Data 1 Pattern Setting Register (Max)	D1PMAX	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B0Eh	RCR0	Special Data Pattern Setting Register (Min)	SDPMIN	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B10h	RCR0	Special Data Pattern Setting Register (Max)	SDPMAX	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B12h	RCR0	Pattern End Setting Register	PE	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B15h	RCR0	Receive Bit Count Register	RBIT	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.

Table 4.1 List of I/O Registers (Address Order) (33 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000A 0B16h	RCR0	Receive Data 0 Register	DAT0	8	8	1 to 2PCLK	1 ICLK	RCR	Not available in 5-V packages.
000A 0B17h	RCR0	Receive Data 1 Register	DAT1	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B18h	RCR0	Receive Data 2 Register	DAT2	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B19h	RCR0	Receive Data 3 Register	DAT3	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B1Ah	RCR0	Receive Data 4 Register	DAT4	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B1Bh	RCR0	Receive Data 5 Register	DAT5	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B1Ch	RCR0	Receive Data 6 Register	DAT6	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B1Dh	RCR0	Receive Data 7 Register	DAT7	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B1Eh	RCR0	Measurement Result Register	TIM	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B80h	RCR1	Function Select Register 0	CON0	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B81h	RCR1	Function Select Register 1	CON1	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B82h	RCR1	Status Register	STS	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B83h	RCR1	Interrupt Control Register	INT	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B84h	RCR1	Compare Control Register	CPC	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B85h	RCR1	Compare Value Setting Register	CPD	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B86h	RCR1	Header Pattern Setting Register (Min)	HDPMIN	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B88h	RCR1	Header Pattern Setting Register (Max)	HDPMAX	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B8Ah	RCR1	Data 0 Pattern Setting Register (Min)	D0PMIN	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B8Bh	RCR1	Data 0 Pattern Setting Register (Max)	D0PMAX	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B8Ch	RCR1	Data 1 Pattern Setting Register (Min)	D1PMIN	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B8Dh	RCR1	Data 1 Pattern Setting Register (Max)	D1PMAX	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B8Eh	RCR1	Special Data Pattern Setting Register (Min)	SDPMIN	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B90h	RCR1	Special Data Pattern Setting Register (Max)	SDPMAX	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B92h	RCR1	Pattern End Setting Register	PE	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.

Table 4.1 List of I/O Registers (Address Order) (34 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000A 0B95h	RCR1	Receive Bit Count Register	RBIT	8	8	1 to 2PCLK	1 ICLK	RCR	Not available in 5-V packages.
000A 0B96h	RCR1	Receive Data 0 Register	DAT0	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B97h	RCR1	Receive Data 1 Register	DAT1	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B98h	RCR1	Receive Data 2 Register	DAT2	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B99h	RCR1	Receive Data 3 Register	DAT3	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B9Ah	RCR1	Receive Data 4 Register	DAT4	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B9Bh	RCR1	Receive Data 5 Register	DAT5	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B9Ch	RCR1	Receive Data 6 Register	DAT6	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B9Dh	RCR1	Receive Data 7 Register	DAT7	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B9Eh	RCR1	Measurement Result Register	TIM	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0C00h	SYSTEM	Main Clock Supply Control Register	MOSCR	8	8	1 to 2PCLK	1 ICLK	Clock Generation Circuit	Not available in 5-V packages.
000A 0C02h	SYSTEM	Main Clock Noise Filter Control Register	MONFCR	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
007F C402h	FLASH	Flash Mode Register	FMODR	8	8	2 to 3 FCLK	2 to 3 ICLK	Flash Memory	
007F C410h	FLASH	Flash Access Status Register	FASTAT	8	8	2 to 3 FCLK	2 to 3 ICLK		
007F C411h	FLASH	Flash Access Error Interrupt Enable Register	FAEINT	8	8	2 to 3 FCLK	2 to 3 ICLK		
007F C412h	FLASH	Flash Ready Interrupt Enable Register	FRDYIE	8	8	2 to 3 FCLK	2 to 3 ICLK		
007F C440h	FLASH	E2 DataFlash Read Enable Register 0	DFLRE0	16	16	2 to 3 FCLK	2 to 3 ICLK		
007F C442h	FLASH	E2 DataFlash Read Enable Register 1	DFLRE1	16	16	2 to 3 FCLK	2 to 3 ICLK		
007F C450h	FLASH	E2 DataFlash P/E Enable Register 0	DFLWE0	16	16	2 to 3 FCLK	2 to 3 ICLK		
007F C452h	FLASH	E2 DataFlash P/E Enable Register 1	DFLWE1	16	16	2 to 3 FCLK	2 to 3 ICLK		
007F FFB0h	FLASH	Flash Status Register 0	FSTATR0	8	8	2 to 3 FCLK	2 to 3 ICLK		
007F FFB1h	FLASH	Flash Status Register 1	FSTATR1	8	8	2 to 3 FCLK	2 to 3 ICLK		
007F FFB2h	FLASH	Flash P/E Mode Entry Register	FENTRYR	16	16	2 to 3 FCLK	2 to 3 ICLK		
007F FFB4h	FLASH	Flash Protection Register	FPROTR	16	16	2 to 3 FCLK	2 to 3 ICLK		
007F FFB6h	FLASH	Flash Reset Register	FRESETR	16	16	2 to 3 FCLK	2 to 3 ICLK		
007F FFBAh	FLASH	FCU Command Register	FCMDR	16	16	2 to 3 FCLK	2 to 3 ICLK		
007F FFC8h	FLASH	FCU Processing Switching Register	FCPSR	16	16	2 to 3 FCLK	2 to 3 ICLK		
007F FFCAh	FLASH	E2 DataFlash Blank Check Control Register	DFLBCCNT	16	16	2 to 3 FCLK	2 to 3 ICLK		
007F FFCCh	FLASH	Flash P/E Status Register	FPESTAT	16	16	2 to 3 FCLK	2 to 3 ICLK		
007F FFCEh	FLASH	E2 DataFlash Blank Check Status Register	DFLBCSTAT	16	16	2 to 3 FCLK	2 to 3 ICLK		
007F FFE8h	FLASH	Peripheral Clock Notification Register	PCKAR	16	16	2 to 3 FCLK	2 to 3 ICLK		

Note: This table lists the I/O registers in both 5-V and 3-V package specifications. The I/O registers of each product correspond to the functions listed in Table 1.2. For details, see Table 1.2, Comparison of Functions of Different RX634 Group Products.
Note: The CEC, RCR0, and RCR1 are not available in 5-V packages.
Note 1. Odd addresses cannot be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMR0 or TMR2 register.
Note 2. Odd addresses cannot be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMOCNTL register.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings
Conditions: VSS = AVSS0 = VREFL = VREFL0 = 0 V

Item	Symbol	Value	Unit
Power supply voltage	VCC	–0.3 to +6.5	V
Analog power supply voltage	AVCC0*1	–0.3 to +6.5	V
Reference power supply voltage	VREFH0*1	–0.3 to AVCC0 + 0.3	V
	VREFH*1	–0.3 to +6.5	V
Input voltage (except for port 4, ports 03, 05, and 07)	V_{in}	–0.3 to VCC + 0.3	V
Input voltage (port 4, port 07)	V_{in}	–0.3 to AVCC0 + 0.3	V
Input voltage (ports 03, 05)	V_{in}	–0.3 to VREFH + 0.3	V
Analog input voltage (ports 4, E)	V_{AN}	–0.3 to AVCC0 + 0.3	V
Operating temperature	T_{opr}	–40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.
To preclude any malfunctions due to noise interferences, insert capacitors of high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, and between the VREFH0 and VREFL0 pins. Place capacitors of 0.1 µF or so as close to every power pin and use the shortest and heaviest possible traces.

Note 1. When neither the A/D converter nor the D/A converter is in use, do not leave the AVCC0, VREFH/VREFH0, AVSS0, and VREFL/VREFL0 pins open. Connect the AVCC0 and VREFH/VREFH0 pins to VCC, and the AVSS0 and VREFL/VREFL0 pins to VSS, respectively.

5.2 DC Characteristics

Table 5.2 DC Characteristics (1)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RIIC input pin (except for SMBus)	V_{IH}	VCC × 0.7	—	VCC + 0.3	V	
	Port 4, port 07		AVCC0 × 0.8	—	AVCC0 + 0.3		
	Ports 03, 05		VREFH × 0.8	—	VREFH + 0.3		
	Port L5		VCC × 0.8	—	3.9		Conditions 1
	Except for RIIC input pin, port 4, ports 03, 05, 07, port L5		VCC × 0.8	—	VCC + 0.3		
	RIIC input pin (except for SMBus)	V_{IL}	–0.3	—	VCC × 0.3		
	Port 4, port 07		–0.3	—	AVCC0 × 0.2		
	Port 03, 05		–0.3	—	VREFH × 0.2		
	Port L5		–0.3	—	VCC × 0.2		Conditions 1
	Except for RIIC input pin, port 4, ports 03, 05, 07, port L5		–0.3	—	VCC × 0.2		
	RIIC input pin (except for SMBus)	ΔV_T	VCC × 0.05	—	—		
	Port 4, port 07		AVCC0 × 0.06	—	—		
	Ports 03, 05		VREFH × 0.06	—	—		
	Port L5		VCC × 0.06	—	—		Conditions 1
	Except for RIIC input pin, port 4, ports 03, 05, 07, port L5		VCC × 0.06	—	—		
Input level voltage (except for schmitt trigger input pins)	MD, EMLE	V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	EXTAL, WAIT#, TCK, RSPI input pin		VCC × 0.8	—	VCC + 0.3		
	D0 to D15		VCC × 0.7	—	VCC + 0.3		
	RIIC input pin (SMBus)		2.1	—	VCC + 0.3		Conditions 1
	CEC input pin		2.0	—	3.9		Conditions 1
	MD, EMLE	V_{IL}	–0.3	—	VCC × 0.1		
	EXTAL, WAIT#, TCK, RSPI input pin		–0.3	—	VCC × 0.2		
	D0 to D15		–0.3	—	VCC × 0.3		
	RIIC input pin (SMBus)		–0.3	—	0.8		Conditions 1
	CEC input pin		–0.3	—	0.8		Conditions 1
	CEC input pin	ΔV_T	—	0.3	—		Conditions 1

Table 5.3 DC Characteristics (2)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item			Symbol	Min.	Typ.	Max.	Test Conditions
Input leakage current	RES#, MD input pin, P35/NMI, EXTAL, port 4	$\lvert I_{in} \rvert$	—	—	1.0	μA	V_{in} = 0 V, VCC
Three-state leakage current (off-state)	Ports 12, 13, 16, 17, 20, 21, C0, C1	$\lvert I_{TSI} \rvert$	—	—	5.0	μA	V_{in} = 0 V, VCC
	Except for ports 12, 13, 16, 17, 20, 21, C0, C1		—	—	1.0		
	Port L5		—	—	1.8		VCC = 0 V, V_{in} = 3.9 V
Input capacitance	All input pins (except for ports 12, 13, 16, 17, 20, 21, C0, C1)	C_{in}	—	—	15	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25°C
	Ports 12, 13, 16, 17, 20, 21, C0, C1		—	—	30		

Table 5.4 DC Characteristics (3)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item		Symbol	VCC				Unit	Test Conditions
			2.7 to 3.6V		4.0 to 5.5V			
			Min.	Max.	Min.	Max.		
Input pull-up MOS current	All ports (except for ports 03, 05, ports 35 to P37, port 4, port L5)	I_p	–200	–10	–400	–50	μA	V_{in} = 0 V

Table 5.5 DC Characteristics (4)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 54 MHz	I_{CC}	20	—	mA	ICLK = 54 MHz PCLKB = 27 MHz PCLKD = 54 MHz FCLK = 27 MHz BCLK = 54 MHz
			All peripheral operation: Normal*3	ICLK = 54 MHz		24	—		
			All peripheral operation: Max.*3	ICLK = 54 MHz		—	55		
		Sleep mode	No peripheral operation	ICLK = 54 MHz		15.5	—		
			All peripheral operation: Normal	ICLK = 54 MHz		19.5	—		
		All-module clock stop mode				14	—		
		Increase during BGO operation*4				12	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation.

Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation.

Note 4. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.

Table 5.6 DC Characteristics (5)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Low-speed operating mode 1	Normal operating mode	No peripheral operation*2	ICLK = 1 MHz	I_{CC}	4	—	mA	
			All peripheral operation: Normal*3	ICLK = 1 MHz		4.2	—		
			All peripheral operation: Max.*3	ICLK = 1 MHz		—	15		
		Sleep mode	No peripheral operation	ICLK = 1 MHz		3.8	—		
			All peripheral operation: Normal	ICLK = 1 MHz		4.0	—		
		All-module clock stop mode				3.7	—		
	Low-speed operating mode 2	Normal operating mode	No peripheral operation*4	ICLK = 125 kHz		0.4	—		
			All peripheral operation: Normal*5	ICLK = 125 kHz		0.5	—		
			All peripheral operation: Max.*5	ICLK = 125 kHz		—	8*6		
		Sleep mode	No peripheral operation	ICLK = 125 kHz		0.3	—		
			All peripheral operation: Normal	ICLK = 125 kHz		0.4	—		
		All-module clock stop mode				0.28	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is the main clock.
Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is the main clock.
Note 4. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is LOCO.
Note 5. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is LOCO.
Note 6. Value when the main clock continues oscillating at 13.5 MHz.

Table 5.7 DC Characteristics (6)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item				Symbol	Typ.	Max.	Unit	Test Conditions
Supply power*1	Software standby mode			I_{CC}	40	1000	µA	
	Deep software standby mode	RAM power supplied			22	200		
		RAM power not supplied	Power-on reset circuit low power consumption function disabled		21	60		
			Power-on reset circuit low power consumption function enabled		6.2	28		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Table 5.8 DC Characteristics (7)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Permissible total consumption power*1	Pd	—	360	mW	

Note 1. Total power dissipated by the entire chip (including output currents)

Table 5.9 DC Characteristics (8)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog power supply current	During A/D conversion	I_{AVCC0}	—	1.9	4.2	mA	Conditions 1
			—	2.5	4.2	mA	Conditions 2
	Waiting for A/D conversion		—	0.1	4	μA	
	During D/A conversion (per channel)	I_{VREFH}*1	—	0.3	1	mA	Conditions 1
			—	0.46	1	mA	Conditions 2
	Waiting for A/D, D/A conversion (all units)*2	—	—	23	40	μA	
Reference power supply current	During A/D conversion	I_{VREFH0}	—	0.44	1.5	mA	Conditions 1
			—	0.66	1.5	mA	Conditions 2
	Waiting for A/D conversion		—	0.1	1	μA	

Note: The values for A/D conversion apply when the sample and hold circuit is not in use.
Note 1. The reference power supply current is included in the power supply current value for D/A conversion.
Note 2. The value is the total value of I_{AVCC0} and I_{VREFH}.

Table 5.10 DC Characteristics (9)

Conditions: VCC = AVCC0 = 0 to 5.5 V, VREFH = 0 to AVCC0, VREFH0 = 0 to AVCC0,
VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
VCC rising gradient	SrVCC	—	—	20	ms/V	At cold start

Table 5.11 Permissible Output Currents

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C

Item			Symbol	Max.	Unit
Permissible output low current (average value per 1 pin)		Normal output mode	I_{OL}	2.0	mA
Permissible output low current (maximum value per 1 pin)		Normal output mode		4.0	mA
Permissible output low current (total)	Total of all output pins		ΣI_{OL}	80	mA
Permissible output high current (average value per 1 pin)		Normal output mode	I_{OH}	–2.0	mA
Permissible output high current (maximum value per 1 pin)		Normal output mode		–4.0	mA
Permissible output high current (total)	Total of all output pins		ΣI_{OH}	–80	mA

Table 5.12 Output Values of Voltage (1)

Conditions: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output pins (other than RIIC)	Normal output	V_{OL}	—	0.5	V	I_{OL} = 1.0 mA
		High-drive output		—	0.5		I_{OL} = 2.0 mA
	RIIC pins			—	0.4		I_{OL} = 3.0 mA
				—	0.6		I_{OL} = 6.0 mA
	CEC pins			—	0.6		I_{OL} = 2.1 mA
Output high	All output pins	Normal output	V_{OH}	VCC – 0.5	—	V	I_{OH} = –1.0 mA
		High-drive output		VCC – 0.5	—		I_{OH} = –2.0 mA

Table 5.13 Output Values of Voltage (2)

Conditions: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output pins (other than RIIC)	Normal output	V_{OL}	—	0.8	V	I_{OL} = 2.0 mA
		High-drive output		—	0.8		I_{OL} = 4.0 mA
	RIIC pins			—	0.4		I_{OL} = 3.0 mA
				—	0.6		I_{OL} = 6.0 mA
Output high	All output pins	Normal output	V_{OH}	VCC – 0.8	—	V	I_{OH} = –2.0 mA
		High-drive output		VCC – 0.8	—		I_{OH} = –4.0 mA

5.3 AC Characteristics

Table 5.14 Operation Frequency Value (High-Speed Operating Mode)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit
Operating frequency	System clock (ICLK)	f_{max}	—	—	54	MHz
	FlashIF clock (FCLK)*1		—	—	32	
	Peripheral module clock (PCLKB)		—	—	32	
	Peripheral module clock (PCLKD)*2		—	—	54	
	External bus clock (BCLK)		—	—	54	
	BCLK pin output		—	—	27	

Note 1. The lower-limit frequency of FCLK is 4 MHz during programming or erasing of the flash memory.
Note 2. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

Table 5.15 Operation Frequency Value (Low-Speed Operating Mode 1)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit
Operating frequency	System clock (ICLK)	f_{max}	—	—	1	MHz
	FlashIF clock (FCLK)*1		—	—	1	
	Peripheral module clock (PCLKB)		—	—	1	
	Peripheral module clock (PCLKD)*2		—	—	1	
	External bus clock (BCLK)		—	—	1	
	BCLK pin output		—	—	1	

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

Table 5.16 Operation Frequency Value (Low-Speed Operating Mode 2)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit
Operating frequency	System clock (ICLK)	f_{max}	—	—	143.75	kHz
	FlashIF clock (FCLK)*1		—	—	143.75	
	Peripheral module clock (PCLKB)		—	—	143.75	
	Peripheral module clock (PCLKD)*2		—	—	143.75	
	External bus clock (BCLK)		—	—	143.75	
	BCLK pin output		—	—	143.75	

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The A/D converter cannot be used.

5.3.1 Clock Timing

Table 5.17 BCLK Timing

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	t_{Bcyc}	37	—	—	ns	Figure 5.1
BCLK pin output high pulse width*1	t_{CH}	5	—	—	ns	
BCLK pin output low pulse width*1	t_{CL}	5	—	—	ns	
BCLK pin output rising time	t_{Cr}	—	—	5	ns	
BCLK pin output falling time	t_{Cf}	—	—	5	ns	

Note 1. When the EXTAL external clock input is used with divided by 1 to output from the BCLK pin, the above should be satisfied with a duty cycle of 45 to 55%.

Table 5.18 Clock Timing

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time		t_{EXcyc}	50 (62.5)*1	—	—	ns	Figure 5.2
EXTAL external clock input high pulse width		t_{EXH}	20 (25)*1	—	—	ns	
EXTAL external clock input low pulse width		t_{EXL}	20 (25)*1	—	—	ns	
EXTAL external clock rising time		t_{EXr}	—	—	5	ns	
EXTAL external clock falling time		t_{EXf}	—	—	5	ns	
EXTAL external clock input wait time*2		t_{EXWT}	1	—	—	ms	
Main clock oscillator oscillation frequency*3		f_{MAIN}	8	—	20 (16)*1	MHz	
Main clock oscillation stabilization time (crystal)		$f_{MAINOSC}$	—	—	*3	ms	Figure 5.3
Main clock oscillation stabilization wait time (crystal)		$f_{MAINOSCWT}$	—	—	*4	ms	
LOCO clock cycle time		$t_{LOCOCYC}$	6.96	8	9.4	µs	
LOCO clock cycle time		$t_{LOCOCYC}$	7.27	8	8.89	µs	T_a = 0 to +60°C
LOCO clock oscillation frequency		f_{LOCO}	106.25	125	143.75	kHz	
LOCO clock oscillation frequency		f_{LOCO}	112.5	125	137.5	kHz	T_a = 0 to +60°C
LOCO clock oscillation stabilization wait time		t_{LOCOWT}	—	—	20	µs	Figure 5.4
PLL input frequency		f_{PLLIN}	4	—	20	MHz	
PLL circuit oscillation frequency		t_{LOCOWT}	104	—	200	MHz	
PLL clock oscillation stabilization time	PLL operation started after main clock oscillation has settled	t_{PLL1}	—	—	500	µs	Figure 5.5
PLL clock oscillation stabilization wait time		t_{PLLWT1}	—	—	*5	ms	
PLL clock oscillation stabilization time	PLL operation started before main clock oscillation has settled	t_{PLL2}	—	—	$t_{MAINOSC}$ + t_{PLL1}	ms	Figure 5.6
PLL clock oscillation stabilization wait time		t_{PLLWT2}	—	—	*5	ms	

Note 1. The values in parentheses indicate when the MONFCR register is set to a value other than A5h (noise filter enabled) while CECMCLK is selected as the CEC operating clock and RCRMCLK is selected as the RCR operating clock.
Note 2. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating).
Note 3. When using a main clock, request the oscillator manufacturer to evaluate the oscillator. For the oscillation stabilization time, refer to the evaluation results obtained from the oscillator manufacturer.
Note 4. The number of cycles n selected by the value of the MOSCWTCR.MSTS[4:0] bits determines the main-clock oscillation stabilization waiting time in accord with the formula below.

$$t_{MAINOSCWT} = t_{MAINOSC} + \frac{n + 16384}{f_{MAIN}}$$

Note 5. The number of cycles n selected by the value of the PLLWTCR.PSTS[4:0] bits determines the PLL-clock oscillation stabilization waiting time in accord with the formula below.

$$t_{PLLWT1} = t_{PLL1} + \frac{n + 131072}{f_{PLL}}$$

$$t_{PLLWT2} = t_{PLL2} + \frac{n + 131072}{f_{PLL}} = t_{MAINOSC} + t_{PLL1} + \frac{n + 131072}{f_{PLL}}$$

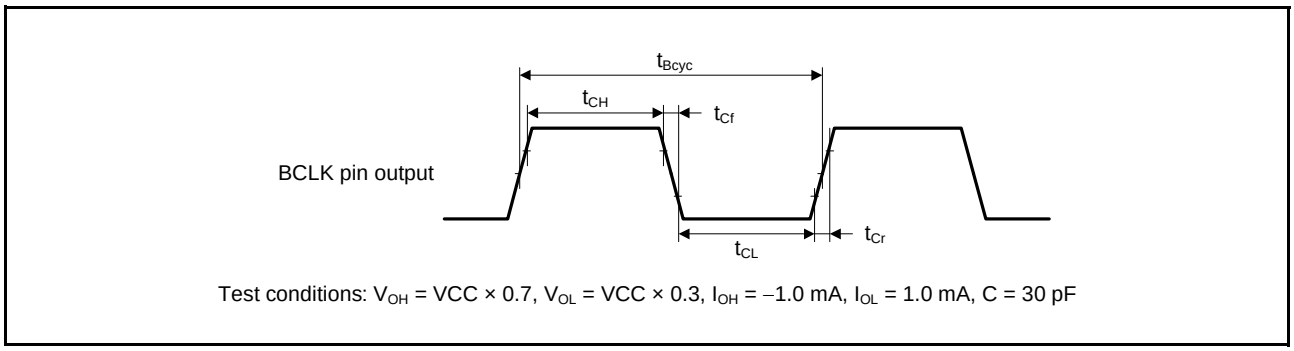


Figure 5.1 BCLK Pin Output Timing

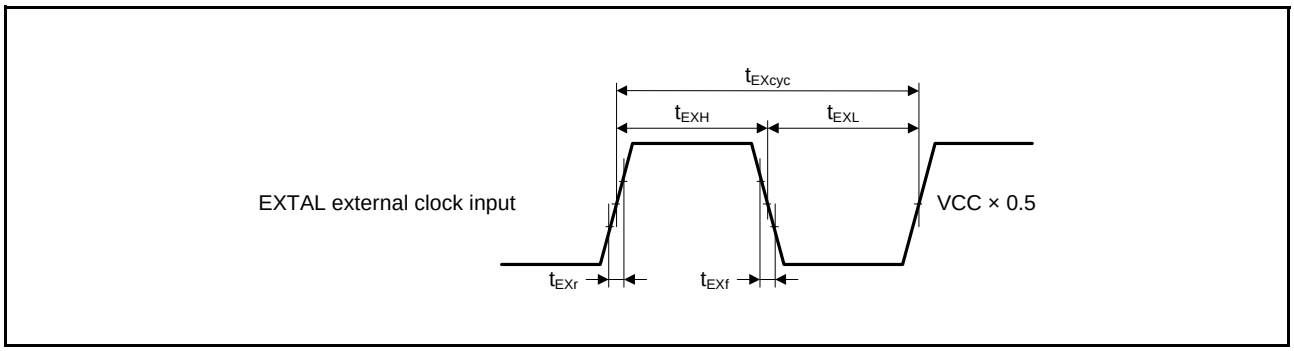


Figure 5.2 EXTAL External Clock Input Timing

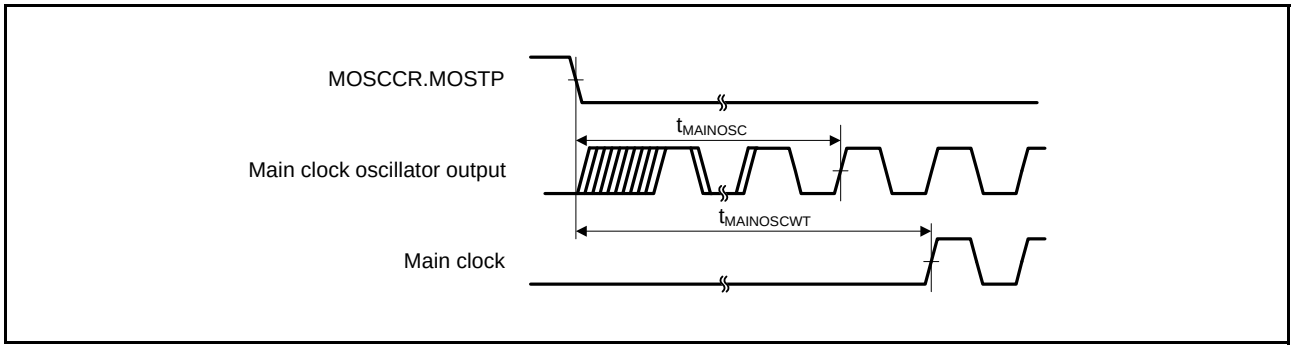


Figure 5.3 Main Clock Oscillation Start Timing

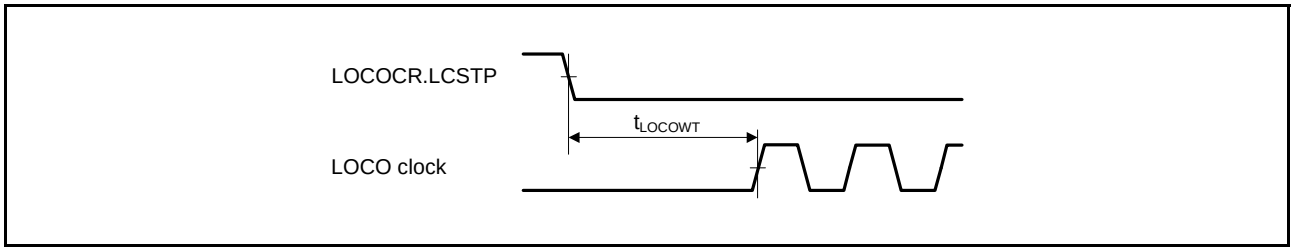


Figure 5.4 LOCO Clock Oscillation Start Timing

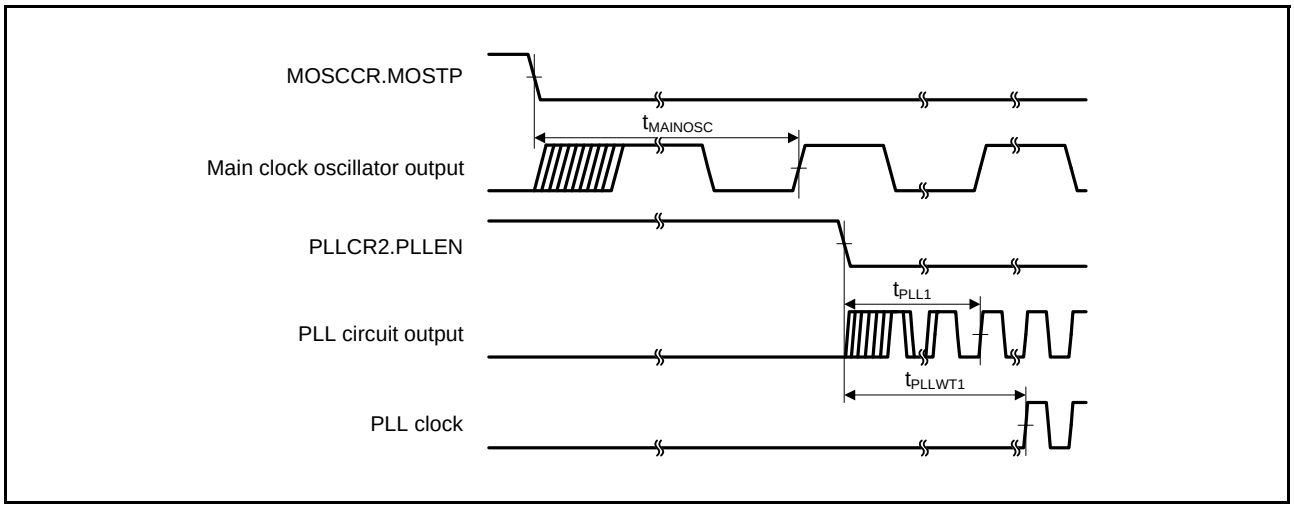


Figure 5.5 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

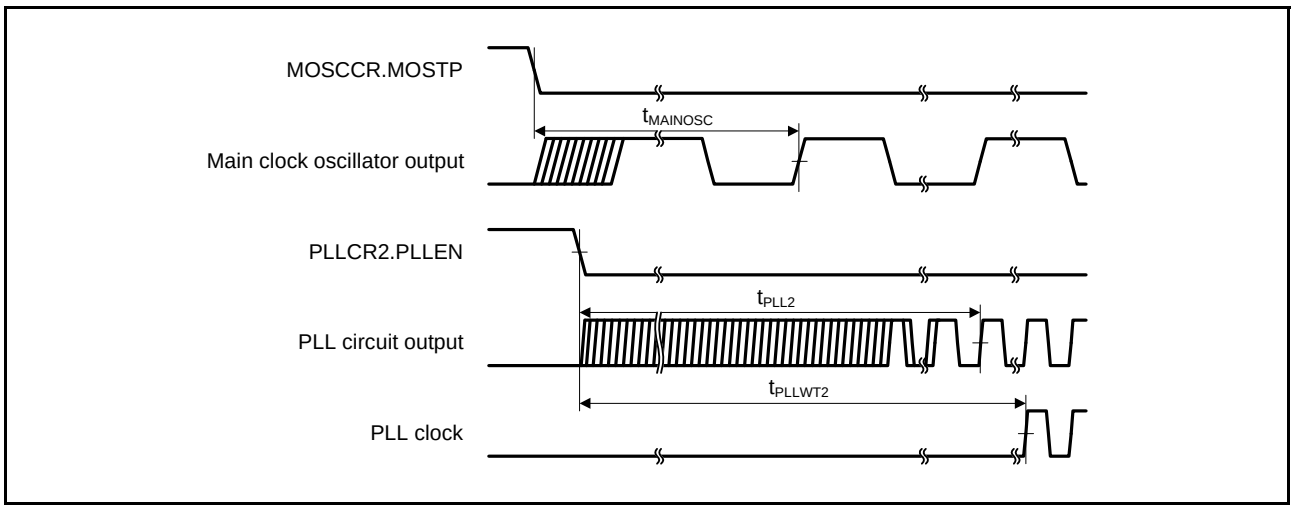


Figure 5.6 PLL Clock Oscillation Start Timing (PLL is Operated before Main Clock Oscillation Has Settled)

5.3.2 Reset Timing

Table 5.19 Reset Timing

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	Power-on	t_{RESWP}	2	—	—	ms	Figure 5.7
	Deep software standby mode	t_{RESWD}	1	—	—	ms	Figure 5.8
	Software standby mode, low-speed operating modes 1 and 2	t_{RESWS}	1	—	—	ms	
	Programming or erasure of the ROM or E2 DataFlash memory or blank checking of the E2 DataFlash memory	t_{RESWF}	200	—	—	µs	
	Other than above	t_{RESW}	200	—	—	µs	
Wait time after RES# cancellation		t_{RESWT}	59	—	60	t_{CYC}	Figure 5.7
Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset)		t_{RESW2}	112	—	120	t_{CYC}	

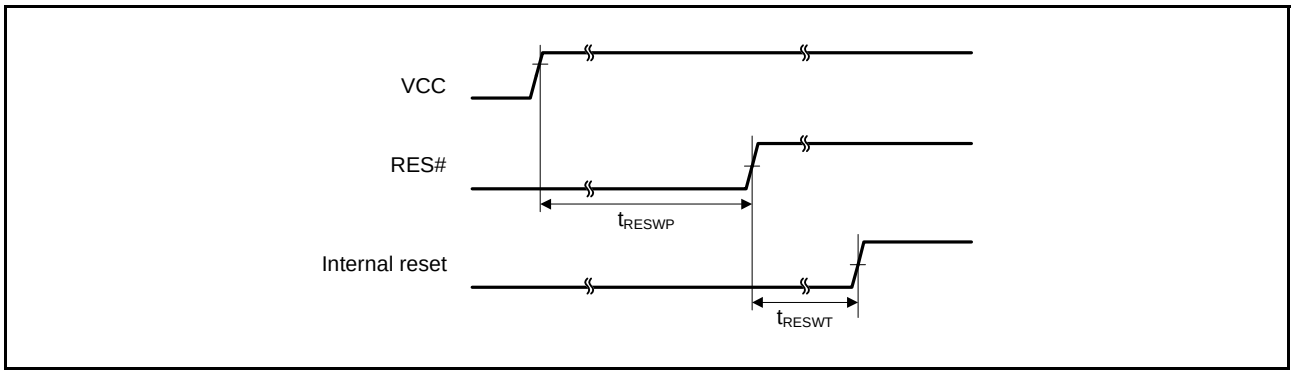


Figure 5.7 Reset Input Timing at Power-On

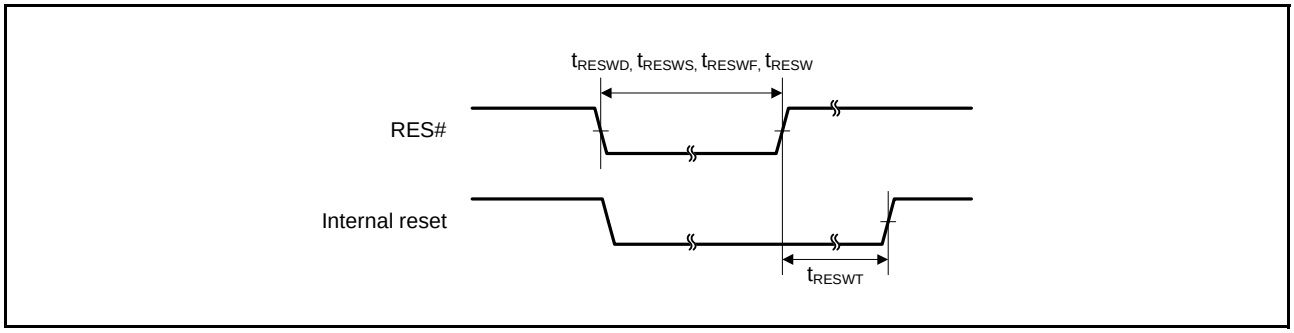


Figure 5.8 Reset Input Timing

5.3.3 Timing of Recovery from Low Power Consumption Modes

Table 5.20 Timing of Recovery from Low Power Consumption Modes

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time after cancellation of software standby mode	Crystal resonator connected to main clock oscillator	Main clock oscillator operating	t_{SBYMC}	10	—	—	ms	Figure 5.9
		Main clock oscillator and PLL circuit operating	t_{SBYPC}	10	—	—	ms	
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}	1	—	—	ms	
		Main clock oscillator and PLL circuit operating	t_{SBYPE}	1	—	—	ms	
	Low-speed on-chip oscillator or IWDT-dedicated on-chip oscillator operating		t_{SBYLO}	—	—	800	µs	
Recovery time after cancellation of deep software standby mode			t_{DSBY}	—	—	1	ms	Figure 5.10
Wait time after cancellation of deep software standby mode			t_{DSBYWT}	45	—	46	t_{CYC}	

Note: The wait time varies depending on the state in which each oscillator was when the WAIT instruction was executed. The recovery time when multiple oscillators are operating is the same period as that when the oscillator which requires the longest time of all operating oscillators to recover is operating alone.

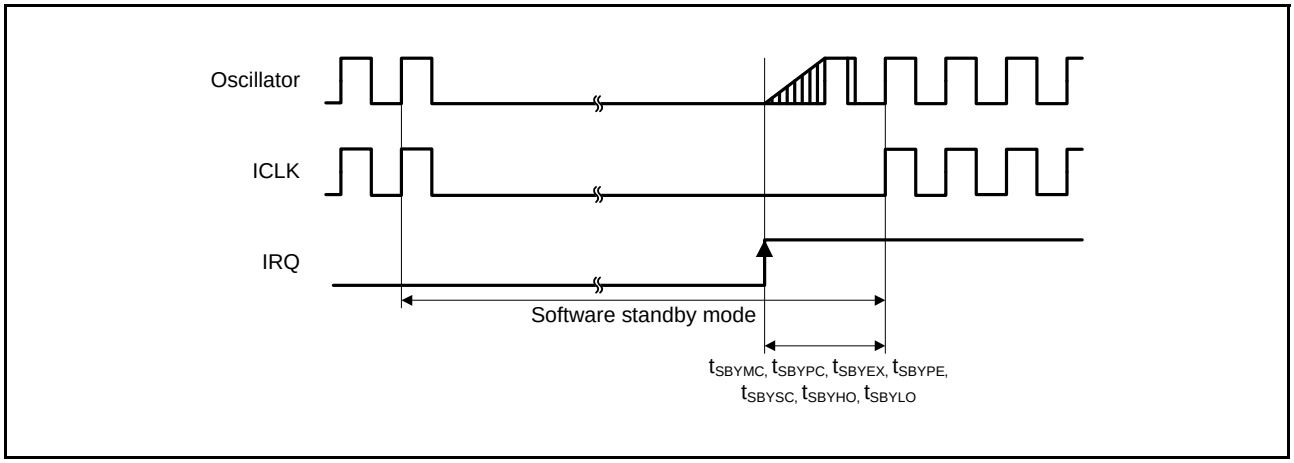


Figure 5.9 Software Standby Mode Cancellation Timing

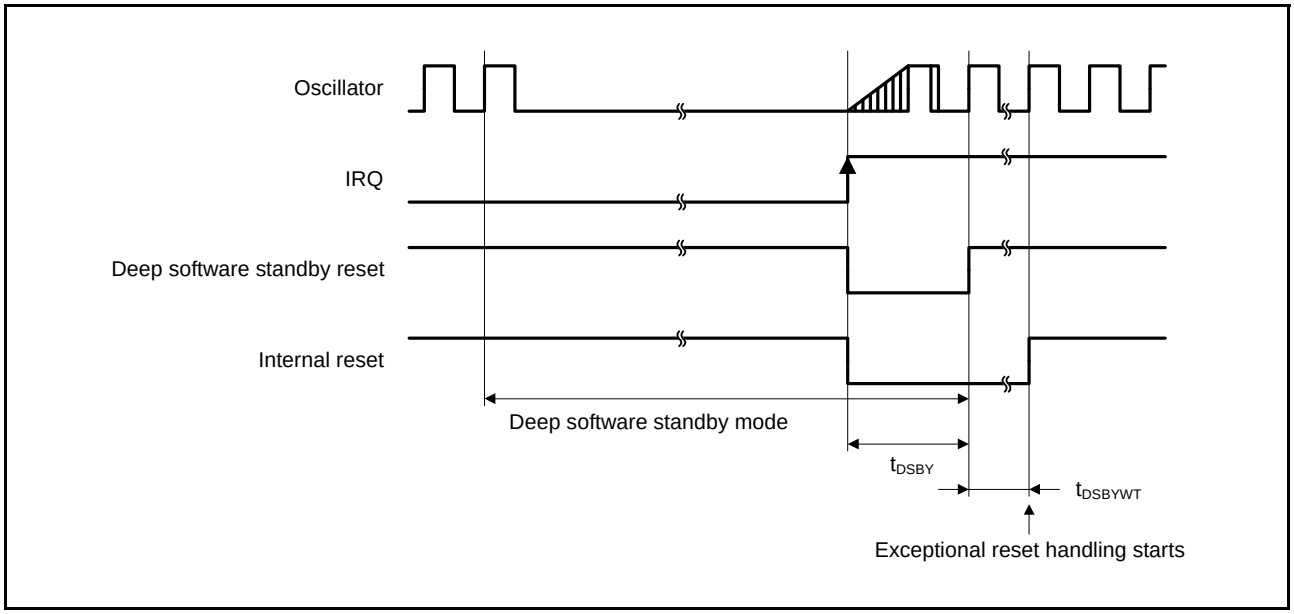


Figure 5.10 Deep Software Standby Mode Cancellation Timing

5.3.4 Control Signal Timing

Table 5.21 Control Signal Timing

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
NMI pulse width	t_{NMIW}	200	—	—	ns	$t_{c\ (PCLKB)}$× 2 ≤ 200ns, Figure 5.11
		$t_{c\ (PCLKB)}$ × 2	—	—	ns	$t_{c\ (PCLKB)}$× 2 > 200ns, Figure 5.11
IRQ pulse width	t_{IRQW}	200	—	—	ns	$t_{c\ (PCLKB)}$× 2 ≤ 200ns, Figure 5.12
		$t_{c\ (PCLKB)}$ × 2	—	—	ns	$t_{c\ (PCLKB)}$× 2 > 200ns, Figure 5.12

Note: 200 ns minimum in deep software standby and software standby modes.

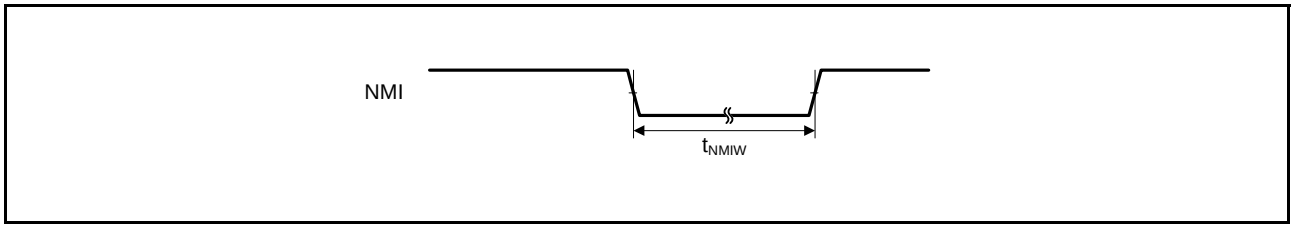


Figure 5.11 NMI Interrupt Input Timing

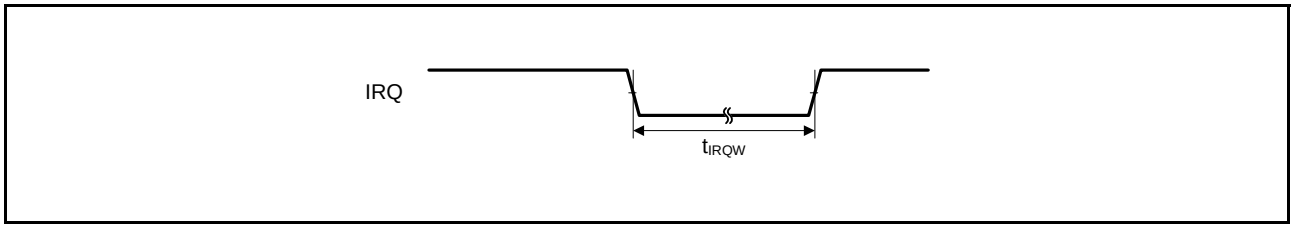


Figure 5.12 IRQ Interrupt Input Timing

5.3.5 Bus Timing

Table 5.22 Bus Timing (1)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C
fBCLK ≤ 54 MHz (BCLK pin output frequency ≤ 27 MHz), VOH = VCC × 0.5, V_{OL} = VCC × 0.5, I_{OH} = –1.0 mA,
I_{OL} = 1.0 mA, CL = 30 pF

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	30	ns	Figure 5.13 to Figure 5.16
Byte control delay time	t_{BCD}	—	30	ns	
CS# delay time	t_{CSD}	—	30	ns	
RD# delay time	t_{RSD}	—	30	ns	
Read data setup time	t_{RDS}	20	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	30	ns	
Write data delay time	t_{WDD}	—	30	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	20	—	ns	Figure 5.17
WAIT# hold time	t_{WTH}	0	—	ns	

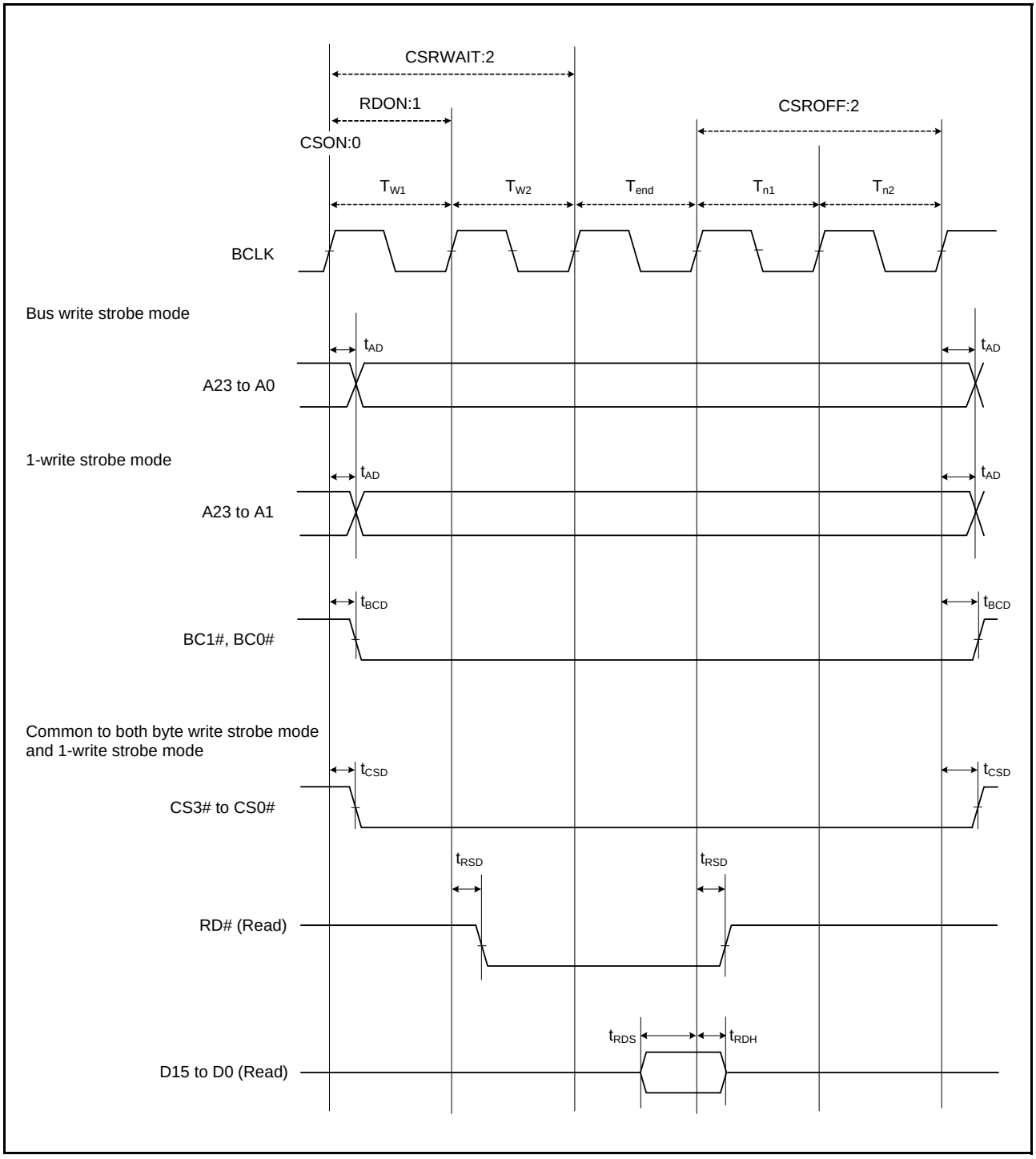
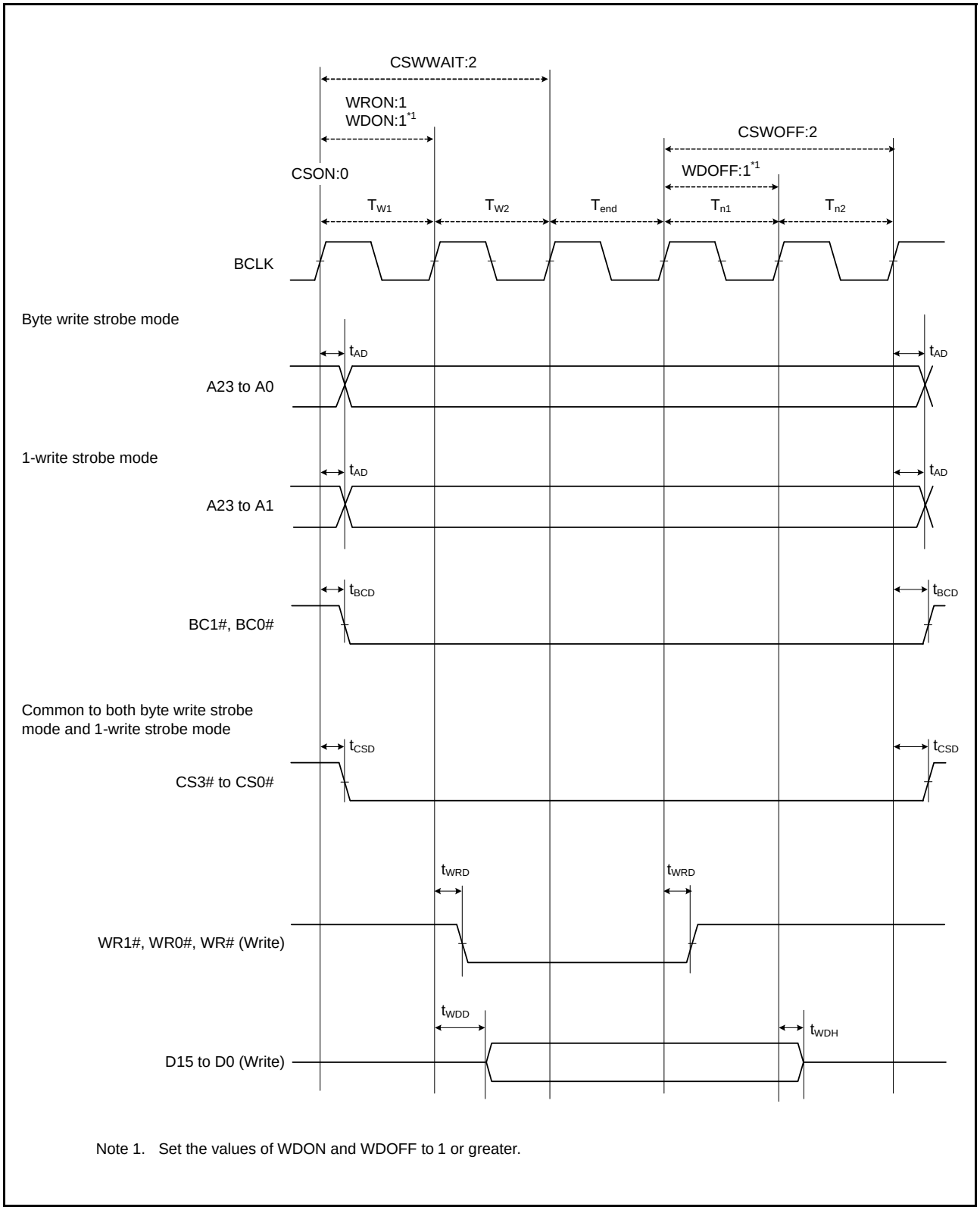


Figure 5.13 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)



Note 1. Set the values of WDON and WDOFF to 1 or greater.

Figure 5.14 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)

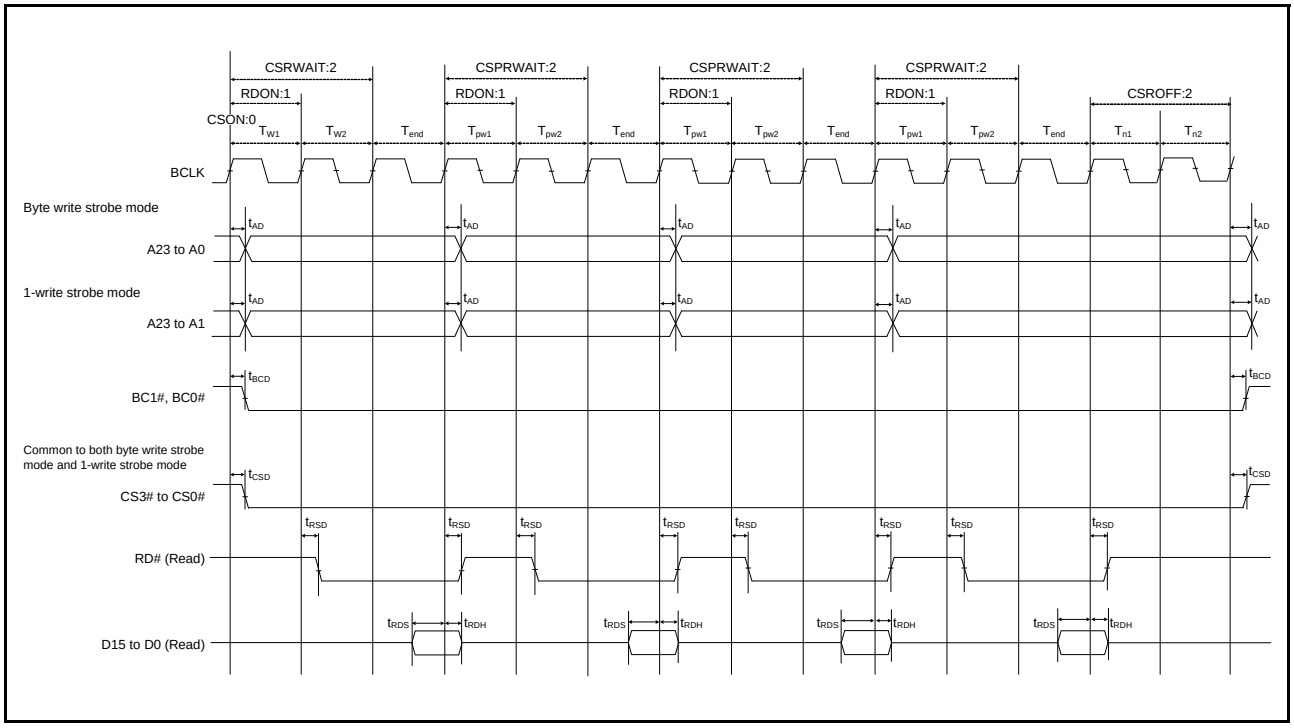
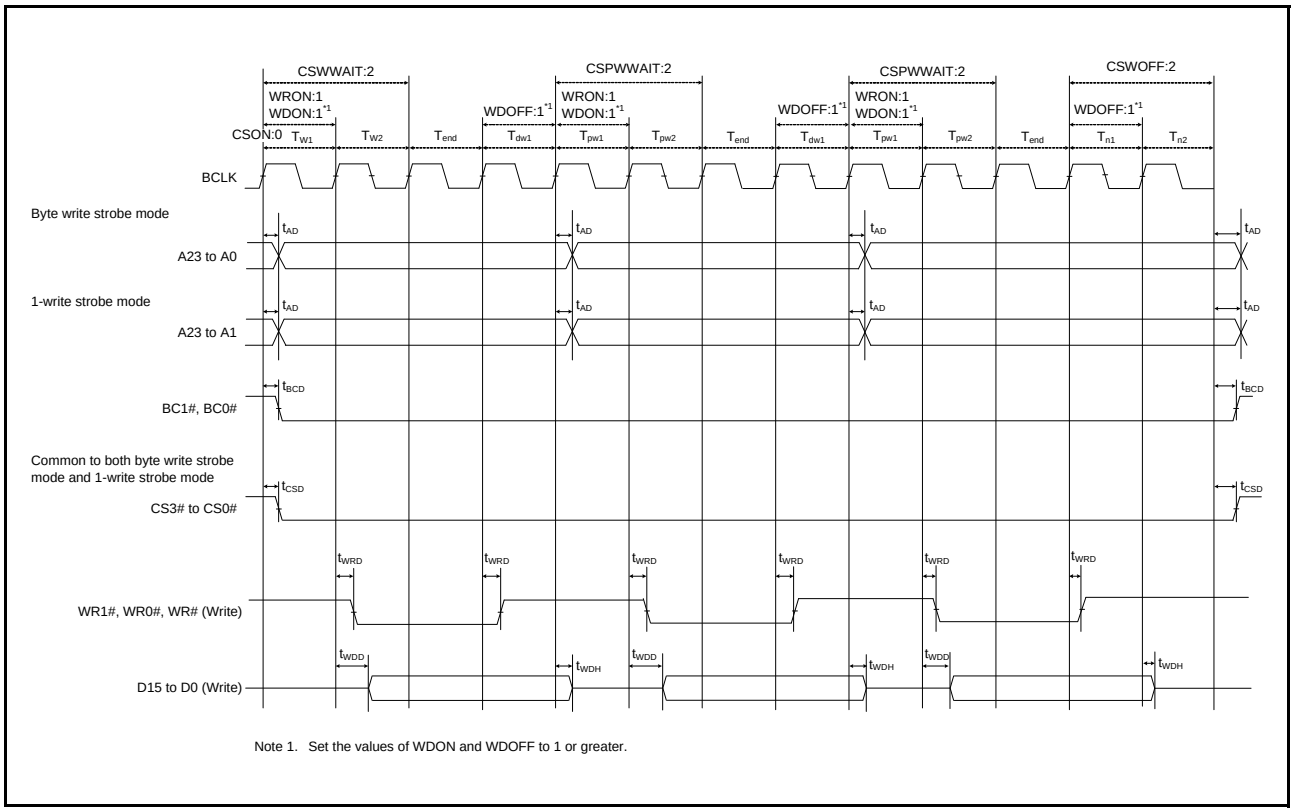


Figure 5.15 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)



Note 1. Set the values of WDON and WDOFF to 1 or greater.

Figure 5.16 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)

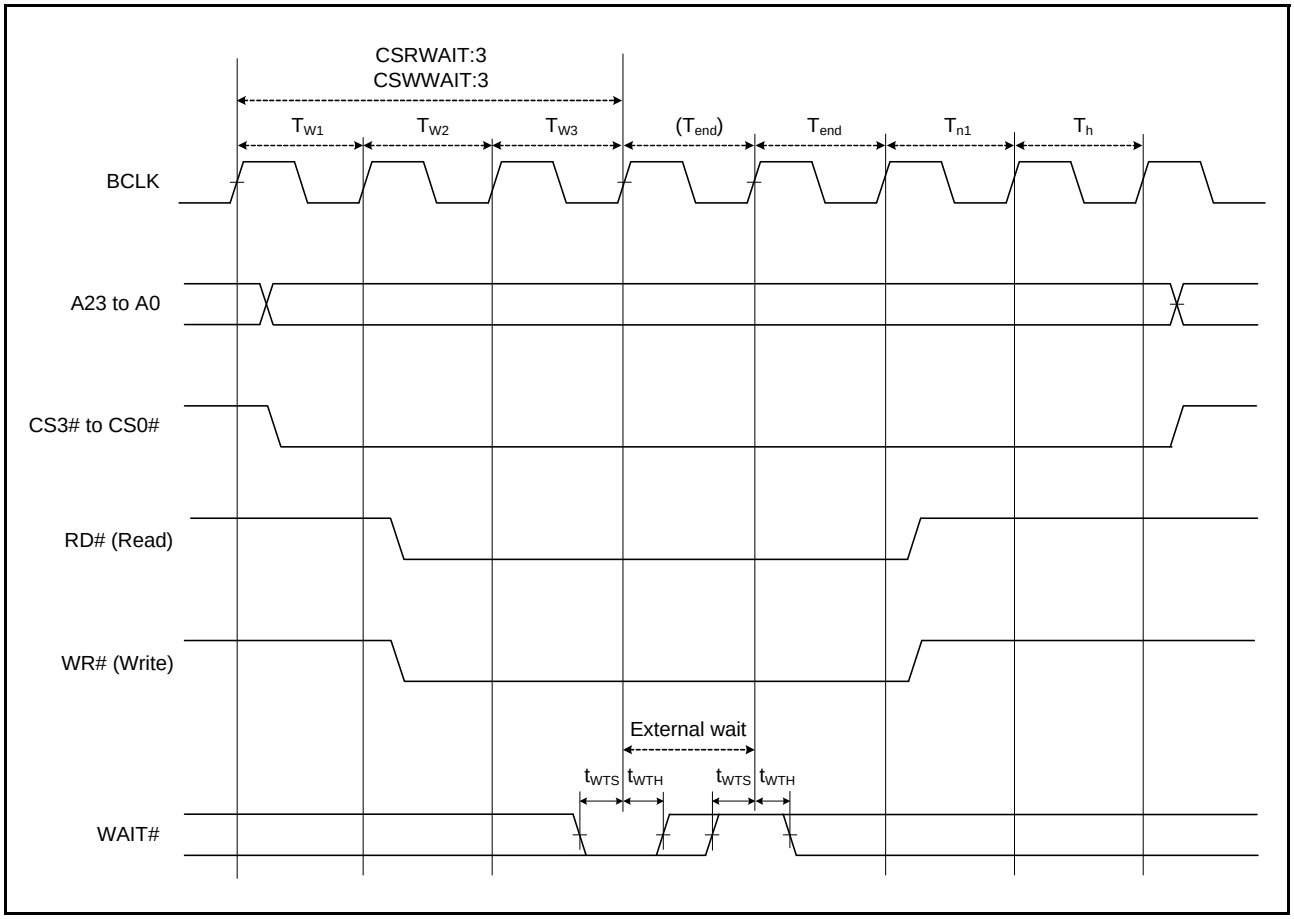


Figure 5.17 External Bus Timing/External Wait Control

Table 5.23 Bus Timing (Multiplexed Bus)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C
fBCLK ≤ 54 MHz (BCLK pin output frequency ≤ 27 MHz), VOH = VCC × 0.5, V_{OL} = VCC × 0.5, I_{OH} = –1.0 mA,
I_{OL} = 1.0 mA, CL = 30 pF

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	30	ns	Figure 5.18, Figure 5.19
Byte control delay time	t_{BCD}	—	30	ns	
CS# delay time	t_{CSD}	—	30	ns	
RD# delay time	t_{RSD}	—	30	ns	
ALE delay time	t_{ALED}	—	30	ns	
Read data setup time	t_{RDS}	20	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	30	ns	
Write data delay time	t_{WDD}	—	30	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	20	—	ns	Figure 5.17
WAIT# hold time	t_{WTH}	0	—	ns	

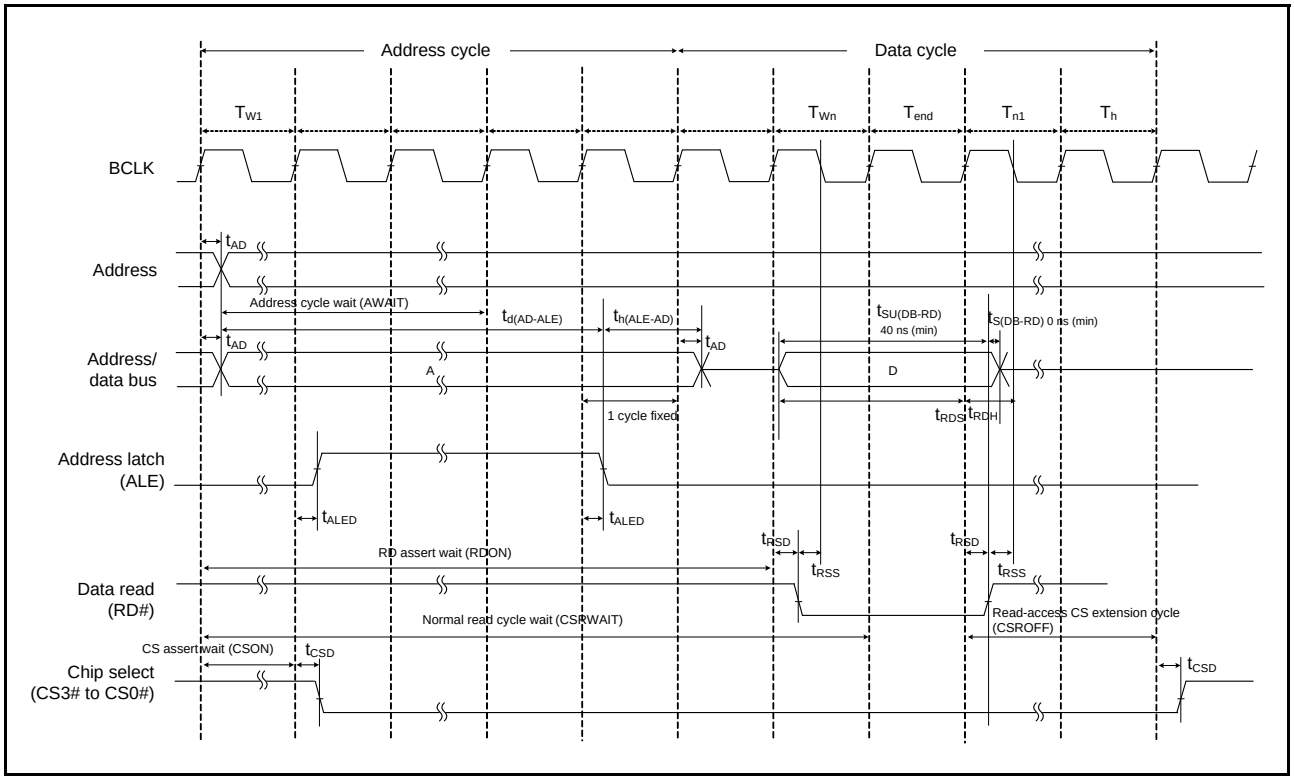


Figure 5.18 Example of Operation in Read Access over the External Bus (Multiplexed)

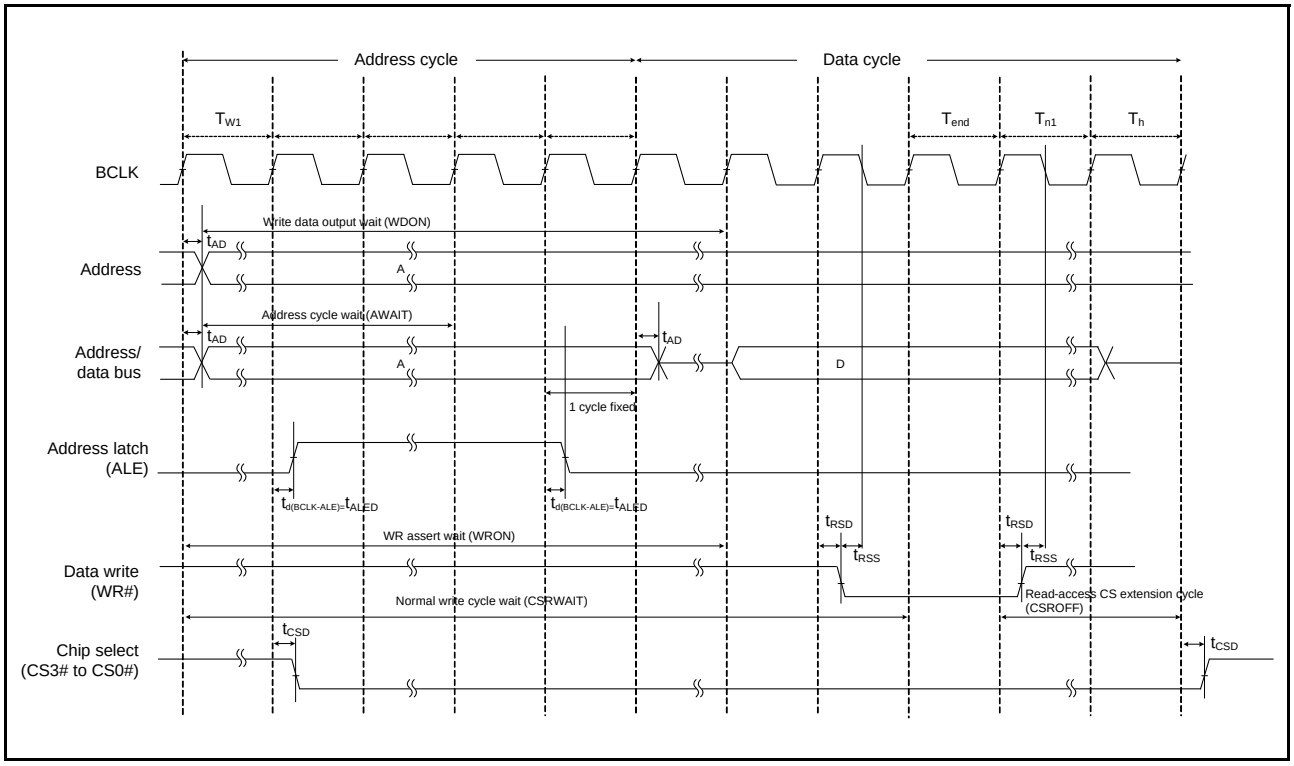


Figure 5.19 Example of Operation in Write Access over the External Bus (Multiplexed)

5.3.6 Timing of On-Chip Peripheral Modules

Table 5.24 Timing of On-Chip Peripheral Modules (1)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C
When high-drive output is selected by the drive capacity control register

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C
When high-drive output is selected by the drive capacity control register

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width		t_{PRW}	1.5	—	t_{Pcyc}	Figure 5.20
MTU/TPU	Input capture input pulse width	Single-edge setting	t_{TICW}	1.5	—	t_{Pcyc}	Figure 5.21
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge setting	t_{TCKWH}, t_{TCKWL}	1.5	—	t_{Pcyc}	Figure 5.22
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		
POE	POE# input pulse width		t_{POEW}	1.5	—	t_{Pcyc}	Figure 5.23
TMR	Timer clock pulse width	Single-edge setting	t_{TMCWH}, t_{TMCWL}	1.5	—	t_{Pcyc}	Figure 5.24
		Both-edge setting		2.5	—		
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	Figure 5.25
		Clock synchronous		6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	20	ns	
	Input clock fall time		t_{SCKf}	—	20	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	16	—	t_{Pcyc}	Figure 5.26
		Clock synchronous		4	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	20	ns	
	Output clock fall time		t_{SCKf}	—	20	ns	
	Transmit data delay time	Clock synchronous	t_{TXD}	—	40	ns	
	Receive data setup time	Clock synchronous	t_{RXS}	40	—	ns	
	Receive data hold time	Clock synchronous	t_{RXH}	40	—	ns	
A/D converter	Trigger input pulse width		t_{TRGW}	1.5	—	t_{Pcyc}	Figure 5.27
CAC	CACREF input pulse width	$t_{Pcyc} \le t_{cac}$*2	t_{CACREF}	4.5 t_{cac} + 3 t_{Pcyc}	—	ns	
		$t_{Pcyc} > t_{cac}$*2		5 t_{cac} + 6.5 t_{Pcyc}	—	ns	

Note 1. t_{Pcyc}: PCLKB cycle
Note 2. t_{cac}: CAC count clock source cycle

Table 5.25 Timing of On-Chip Peripheral Modules (2)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C
When high-drive output is selected by the drive capacity control register

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C
When high-drive output is selected by the drive capacity control register

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}	Figure 5.28
		Slave			8	4096		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/ fall time	Output		t_{SPCKr}, t_{SPCKf}	—	5	ns	
		Input			—	1	µs	
	Data input setup time	Master		t_{SU}	15	—	ns	Figure 5.29 to Figure 5.34
		Slave			$20 - t_{Pcyc}$	—		
	Data input hold time	Master	PCLKB set to a division ratio other than divided by 2	t_H	t_{Pcyc}	—	ns	
			PCLKB set to divided by 2		0	—		
		Slave			$20 + 2 \times t_{Pcyc}$	—		
	SSL setup time	Master		t_{LEAD}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	Data output delay time	Master		t_{OD}	—	18	ns	
		Slave			—	$3 \times t_{Pcyc} + 40$		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$4 \times t_{Pcyc}$	—		
	MOSI and MISO rise/ fall time	Output		t_{Dr}, t_{Df}	—	5	ns	
		Input			—	1	µs	
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	5	ns	
		Input			—	1	µs	
	Slave access time			t_{SA}	—	4	t_{Pcyc}	Figure 5.33, Figure 5.34
	Slave output release time			t_{REL}	—	3	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLKB cycle

Table 5.26 Timing of On-Chip Peripheral Modules (3)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C
When high-drive output is selected by the drive capacity control register

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C
When high-drive output is selected by the drive capacity control register

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)	t_{SPcyc}	4	65536	t_{Pcyc}	Figure 5.28
	SCK clock cycle input (slave)		8	65536		
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time	t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time	t_{SU}	40	—	ns	Figure 5.29 to Figure 5.34
	Data input hold time	t_H	40	—	ns	
	SS input setup time	t_{LEAD}	6	—	t_{Pcyc}	
	SS input hold time	t_{LAG}	6	—	t_{Pcyc}	
	Data output delay time	t_{OD}	—	40	ns	
	Data output hold time	t_{OH}	–10	—	ns	
	Data rise/fall time	t_{Dr}, t_{Df}	—	20	ns	
	SS input rise/fall time	t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time	t_{SA}	—	5	t_{Pcyc}	Figure 5.33, Figure 5.34
	Slave output release time	t_{REL}	—	5	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLKB cycle

Table 5.27 Timing of On-Chip Peripheral Modules (4)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C

Item		Symbol	Min.(*1, *2)	Max.	Unit	Test Conditions
RIIC (Standard-mode)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	—	ns	Figure 5.35
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast-mode)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	—	ns	
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	20 + 0.1C_b	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 + 0.1C_b	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc}: RIIC internal reference count clock (IICφ) cycle

Note 1. The value in parentheses is used when the ICMR3.NF[1:0] bits are set to 11b while a digital filter is enabled with the ICFER.NFE bits = 1.

Note 2. C_b indicates the total capacity of the bus line.

Table 5.28 Timing of On-Chip Peripheral Modules (5)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C

Item		Symbol	Min.(*1, *2)	Max.*3	Unit	Test Conditions
Simple IIC (Standard-mode)	SCL, SDA input rise time	t_{Sr}	—	1000	ns	Figure 5.35
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 × t_{pcyc}	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple IIC (Fast-mode)	SCL, SDA input rise time	t_{Sr}	20 + 0.1C_b	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 + 0.1C_b	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 × t_{pcyc}	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note 1. The value in parentheses is used when the ICMR3.NF[1:0] bits are set to 11b while a digital filter is enabled with the ICFER.NFE bits = 1.
Note 2. C_b indicates the total capacity of the bus line.
Note 3. t_{Pcyc}: PCLKB cycle

Table 5.29 Timing of On-Chip Peripheral Modules (6)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C

Item	Symbol	Min.	Max.	Unit	Test Conditions
CEC fall time	t_{cf}	—	50	µs	C_b = 1600 pF, R_b = 27 kΩ
					C_b = 7700 pF, R_b = 3 kΩ

Note 1. Cb: Communication line load capacitance; Rb: Communication line external pull-up resistance

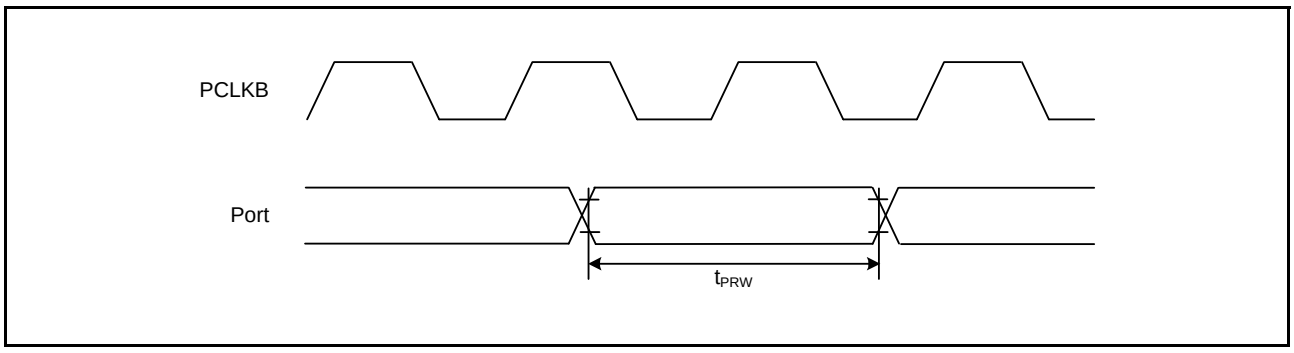


Figure 5.20 I/O Port Input Timing

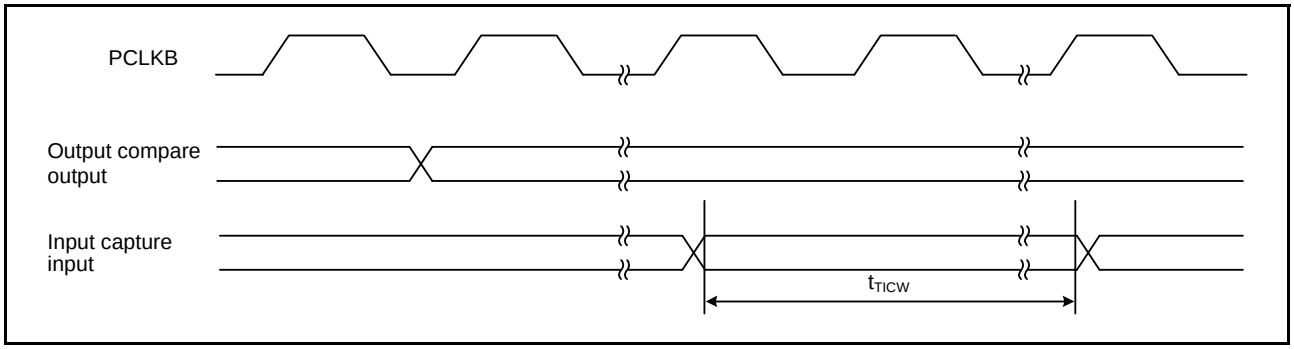


Figure 5.21 MTU/TPU Input/Output Timing

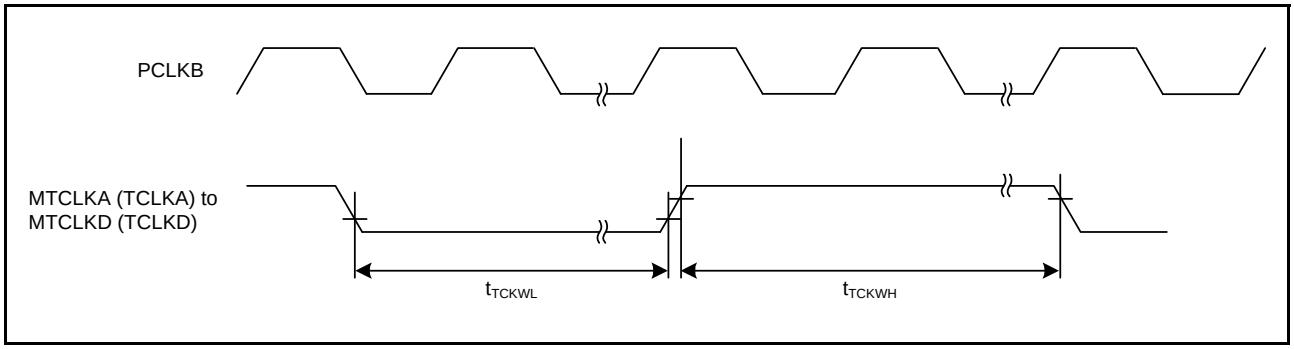


Figure 5.22 MTU/TPU Clock Input Timing

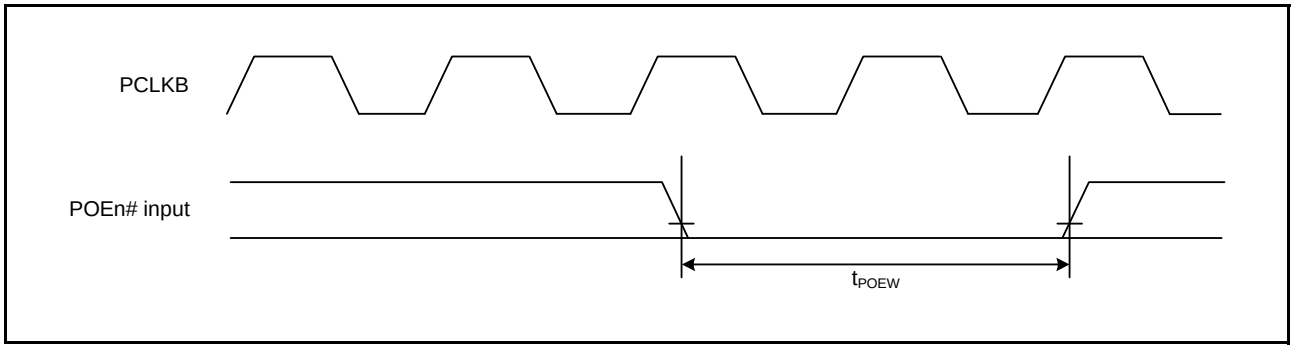


Figure 5.23 POE# Input Timing

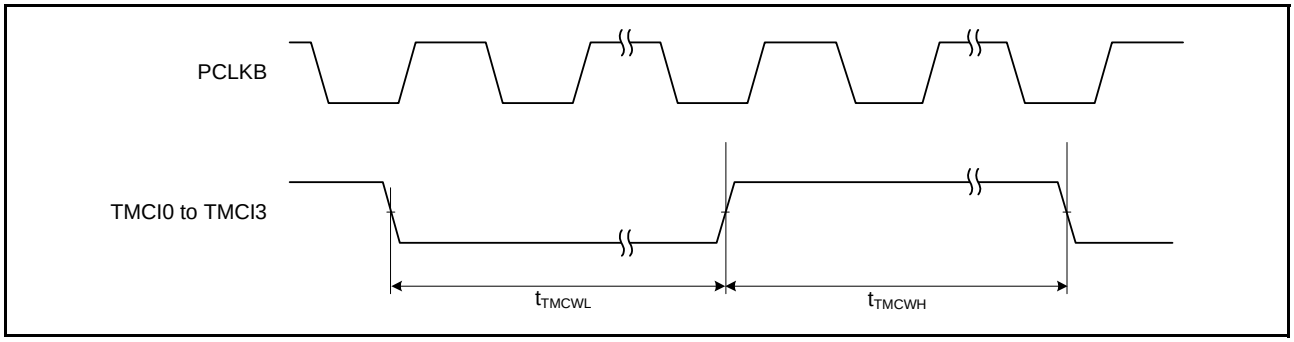


Figure 5.24 8-Bit Timer Clock Input Timing

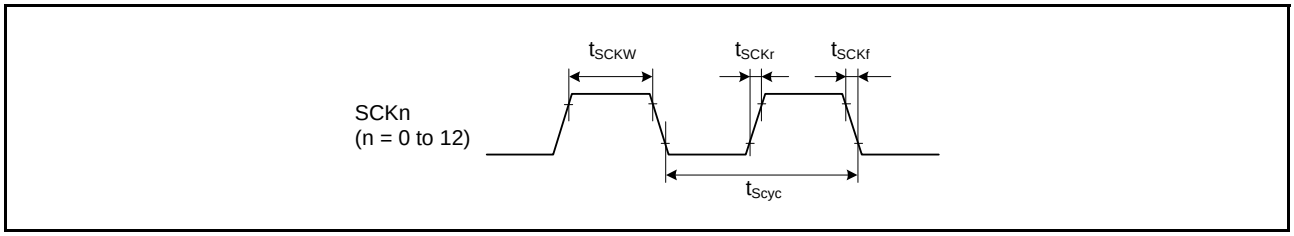


Figure 5.25 SCK Clock Input Timing

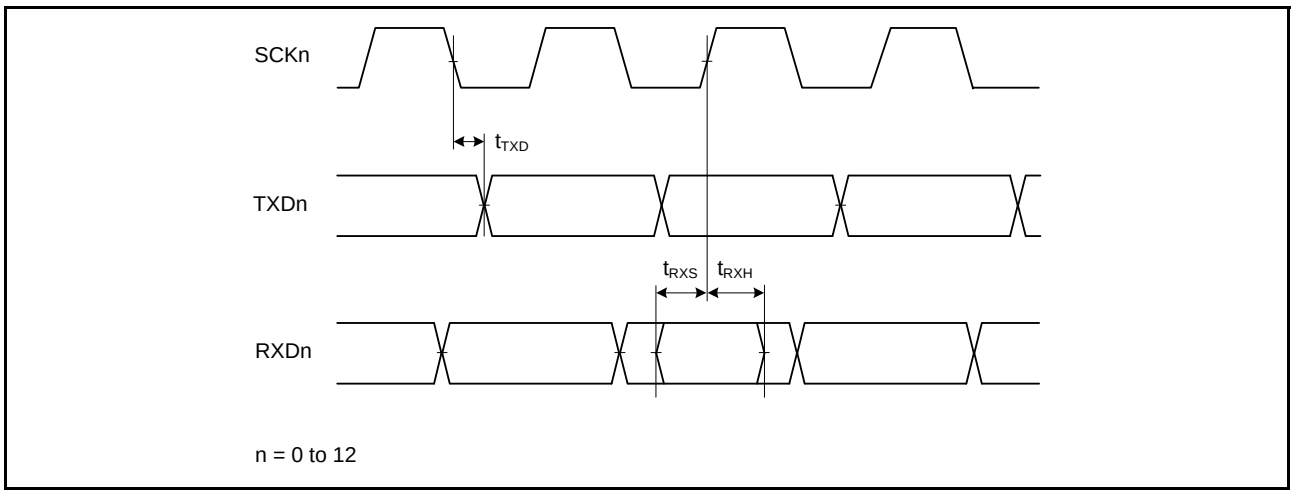


Figure 5.26 SCI Input/Output Timing: Clock Synchronous Mode

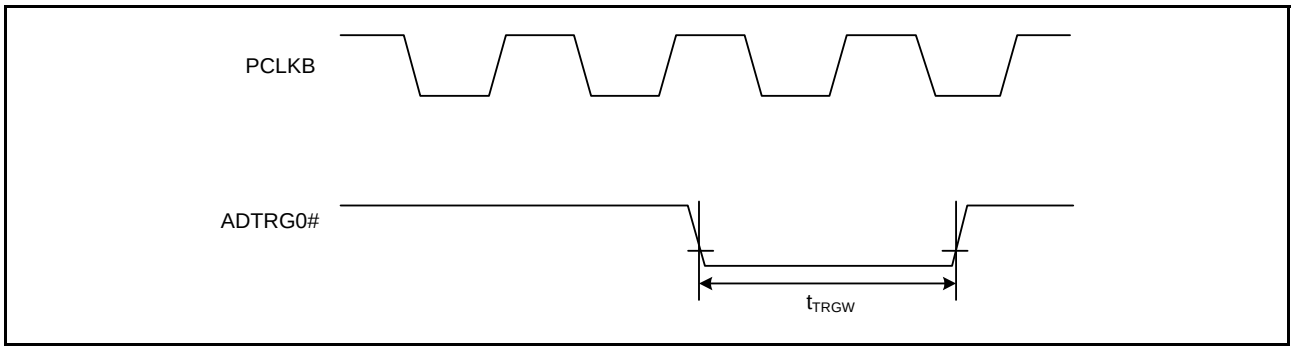


Figure 5.27 A/D Converter External Trigger Input Timing

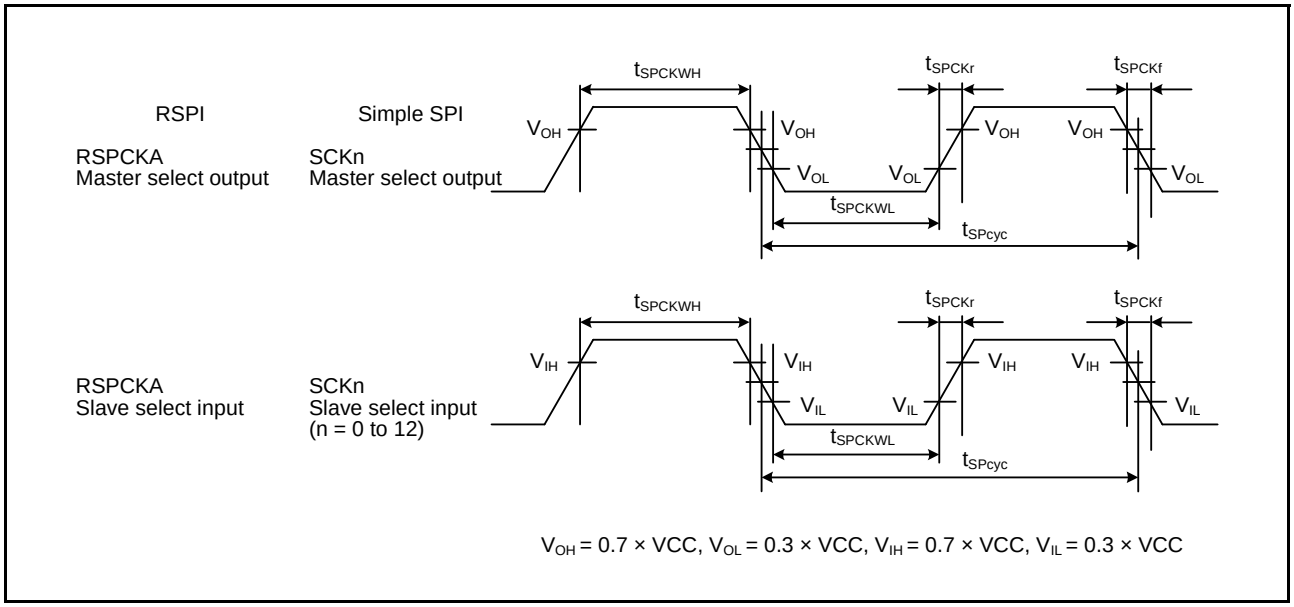


Figure 5.28 RSPI Clock Timing and Simple SPI Clock Timing

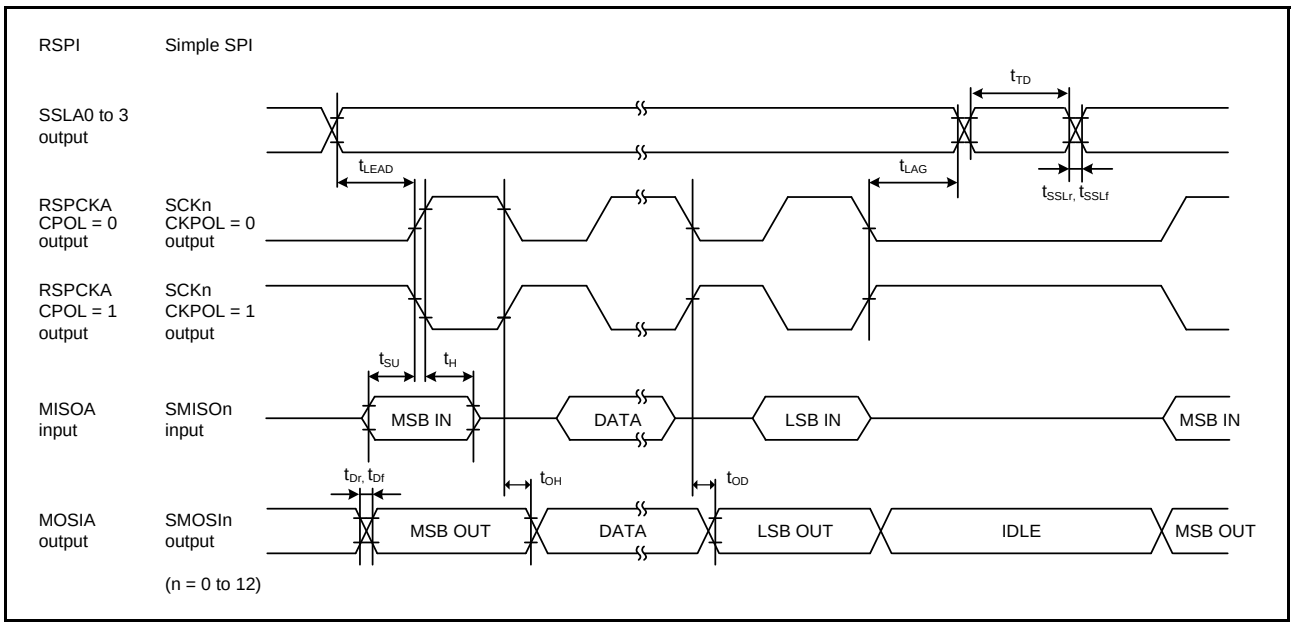


Figure 5.29 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKB Set to Division Ratio Other Than Divided by 2) and Simple SPI Timing (Master, CKPH = 1)

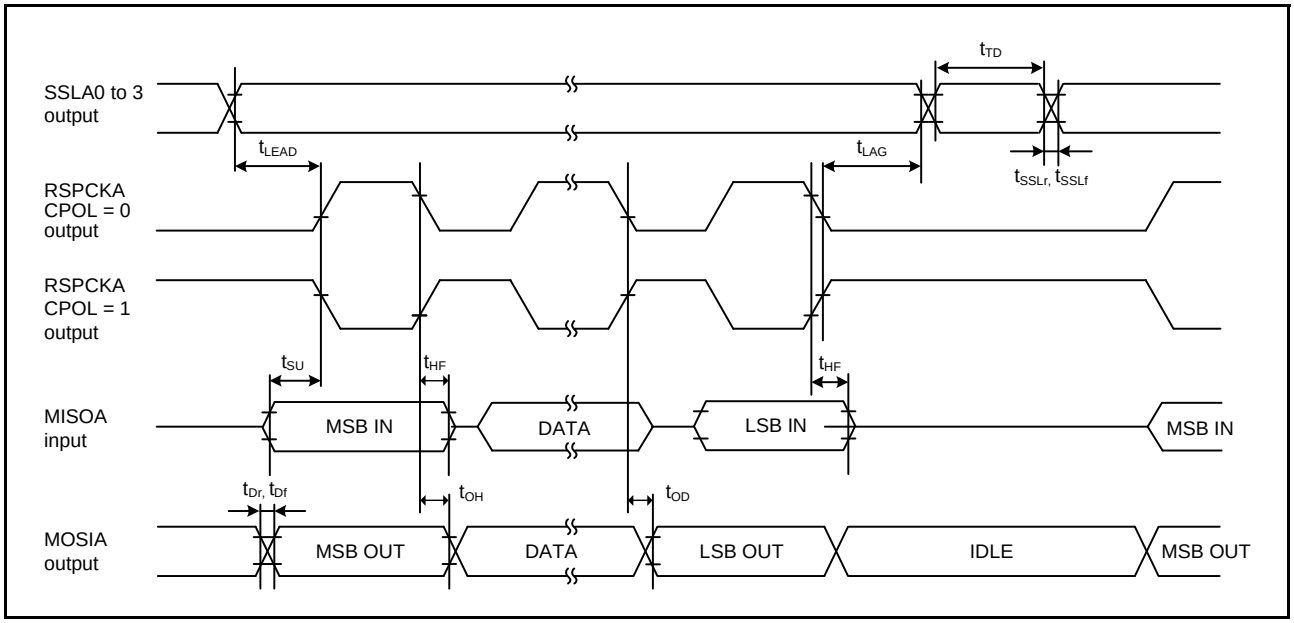


Figure 5.30 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKB Set to Divided by 2)

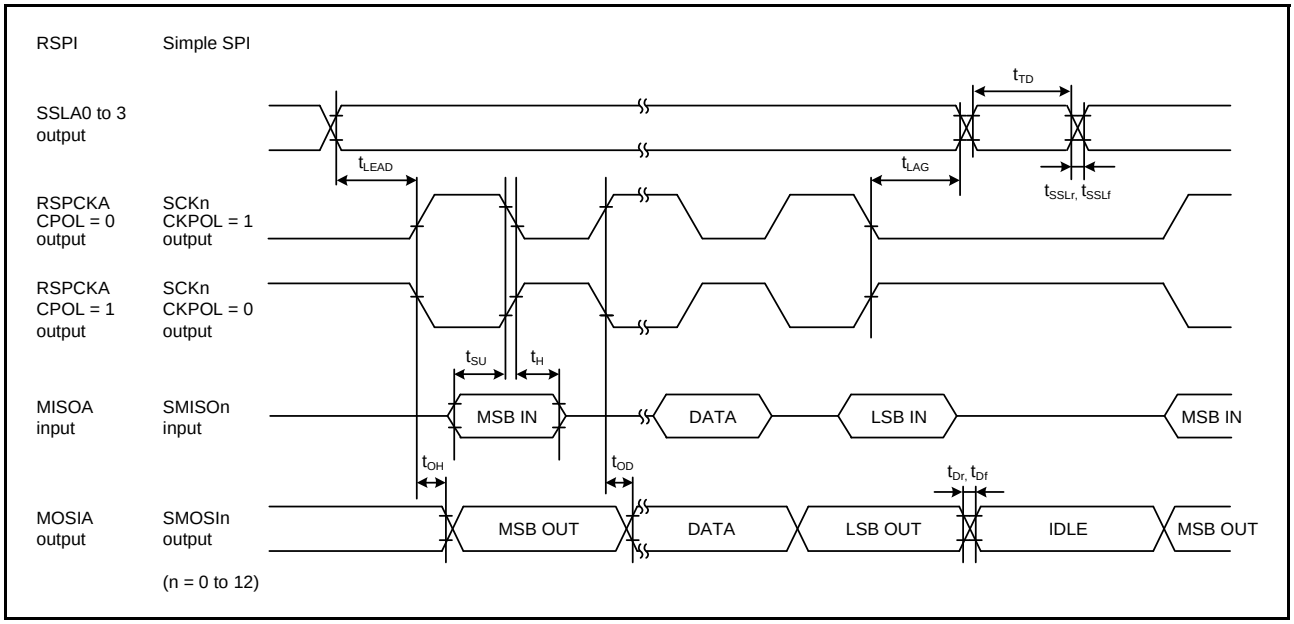


Figure 5.31 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Set to Division Ratio Other Than Divided by 2) and Simple SPI Timing (Master, CKPH = 0)

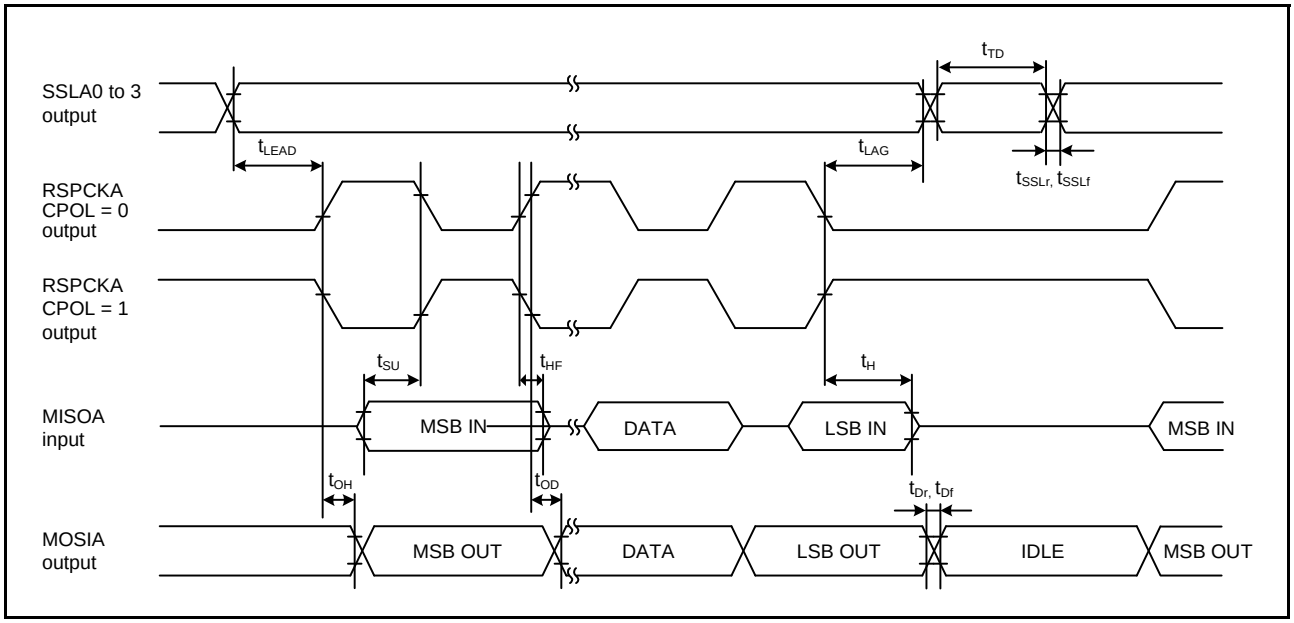


Figure 5.32 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Set to Divided by 2)

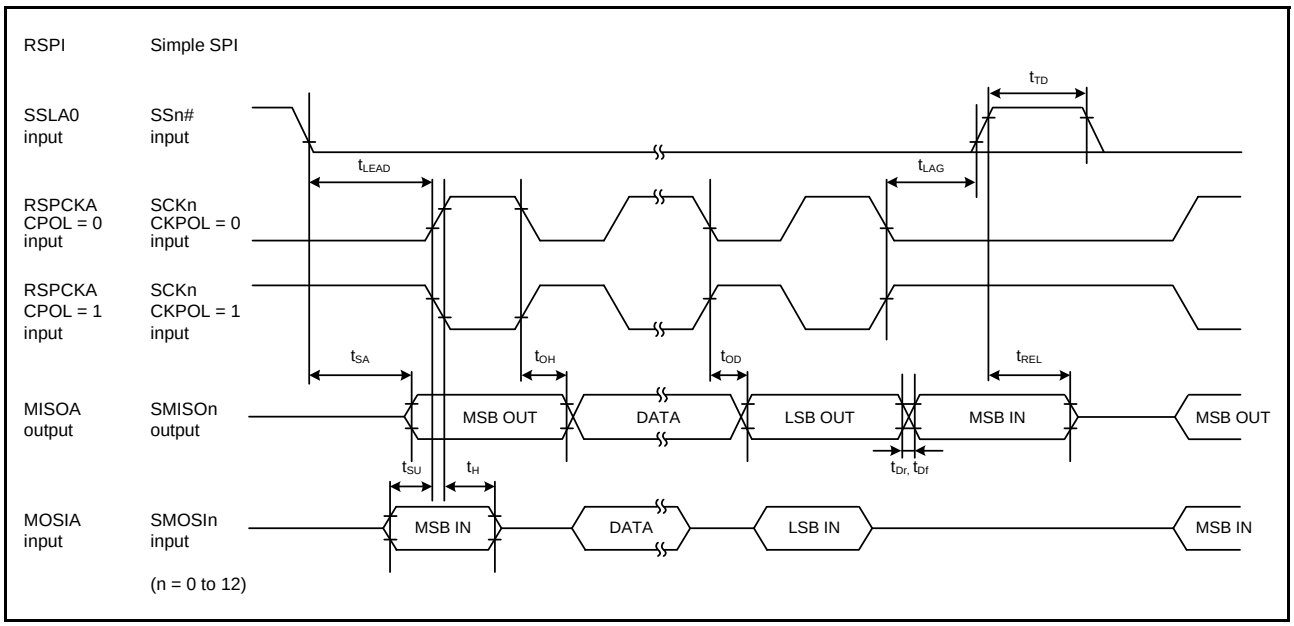


Figure 5.33 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)

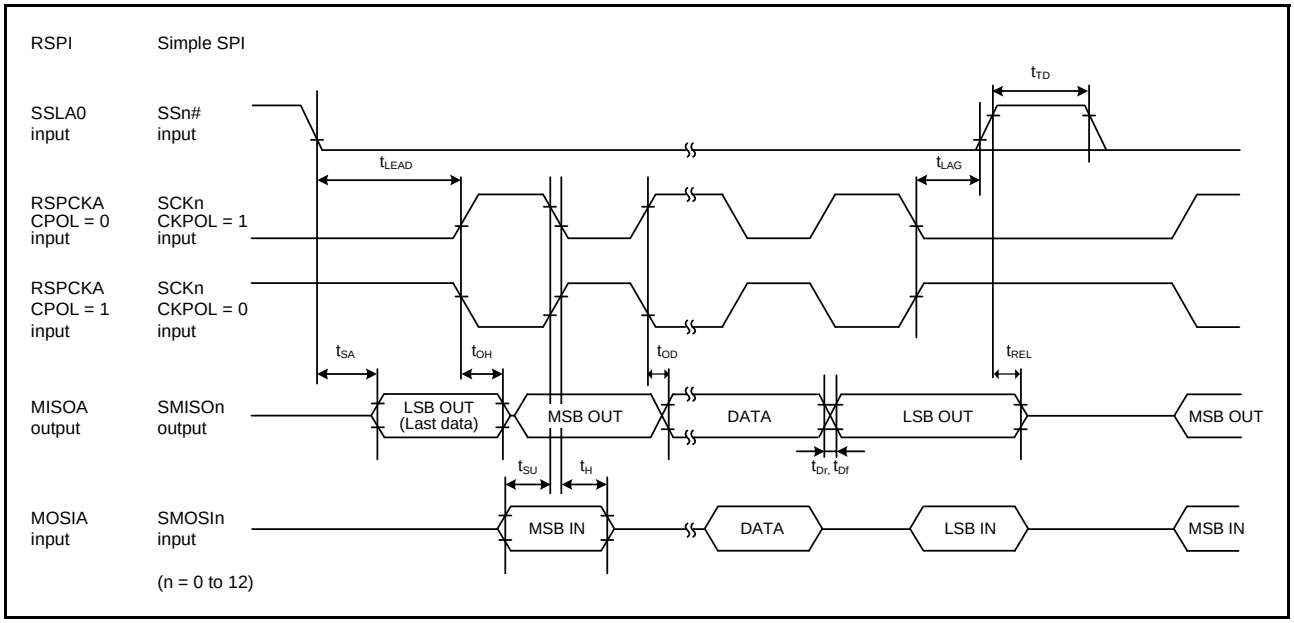
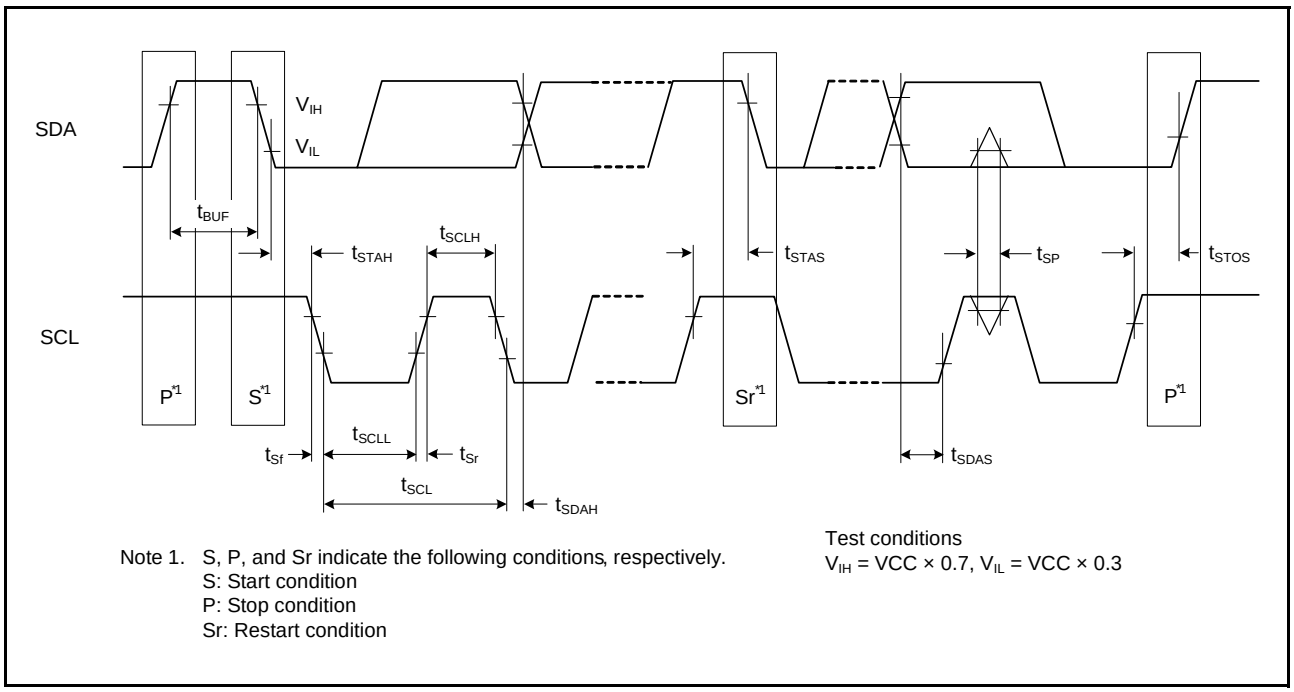


Figure 5.34 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)



Note 1. S, P, and Sr indicate the following conditions, respectively.
S: Start condition
P: Stop condition
Sr: Restart condition

Test conditions
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3

Figure 5.35 RIIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing

5.4 A/D Conversion Characteristics

Table 5.30 A/D Conversion Characteristics

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
A/D conversion clock frequency (fPCLKD)		1	—	54	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (AD clock = 54 MHz)	Permissible signal source impedance = 1.0 kΩ	1 (0.4)*2	—	—	µs	High-precision channel
	Permissible signal source impedance = 1 kΩ, AVCC ≥ 4.0 V	1.9 (1.3)*2	—	—		Normal-precision channel
	Permissible signal source impedance = 1 kΩ, AVCC ≥ 2.7 V	2.5 (1.9)*2	—	—		
Analog input capacitance		—	—	30	pF	
Offset error		—	±2.0	±6.0	LSB	High-precision channel (SH used)
		—	±1.5	±3.0		High-precision channel (SH not used)
		—	±2.0	±7.5		Normal-precision channel
Full-scale error		—	±2.0	±6.0	LSB	High-precision channel (SH used)
		—	±1.5	±3.0		High-precision channel (SH not used)
		—	±2.0	±7.5		Normal-precision channel
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±4.0	±8.0	LSB	High-precision channel (SH used)
		—	±2.0	±6.0		High-precision channel (SH not used)
		—	±2.5	±8.0		Normal-precision channel
DNL differential nonlinearity error		—	±2.0	±6.0	LSB	High-precision channel (SH used)
		—	±1.5	±3.0		High-precision channel (SH not used)
		—	±2.0	±4.0		Normal-precision channel
INL integral nonlinearity error		—	±2.0	±6.0	LSB	High-precision channel (SH used)
		—	±1.5	±3.0		High-precision channel (SH not used)
		—	±2.0	±4.0		Normal-precision channel

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note: When using the channel-dedicated sample-and-hold circuit, use the AN000 to AN002 analog input voltage (V_{AN}) that satisfies all the following conditions: 0.25 V ≤ V_{AN} ≤ AVCC0 - 0.25 V, V_{AN} ≤ VREFH0, and AVCC0 ≥ 2.7 V.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Table 5.31 Sampling Time

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item		Symbol	Typ.	Unit	Test Conditions
Sampling time	High-precision channel	Ts	0.2 + 0.16 × R0 (KΩ)	µs	Figure 5.36
	Normal-precision channel		0.3 + 0.16 × R0 (KΩ)		

Table 5.32 A/D Converter Channel Classification

Classification	Target Channel	Channel-Dedicated Sample-and-Hold Circuit	Condition
High-accuracy channels	AN000 to AN002	Used	AVCC0 = VREFH0 = 2.7 to 3.6V (3-V package) AVCC0 = VREFH0 = 4.0 to 5.5V (5-V package) AVSS0 = VREFL0 = 0V 0.25V ≤ V_{AN} ≤ AVCC0 – 0.25V V_{AN} ≤ VREFH0
		Not used	AVCC0 = VREFH0 = 2.7 to 3.6V (3-V package) AVCC0 = VREFH0 = 4.0 to 5.5V (5-V package) AVSS0 = VREFL0 = 0V 0V ≤ V_{AN} ≤ VREFH0
	AN003 to AN007	—	
Normal-accuracy channels	AN008 to AN015	—	

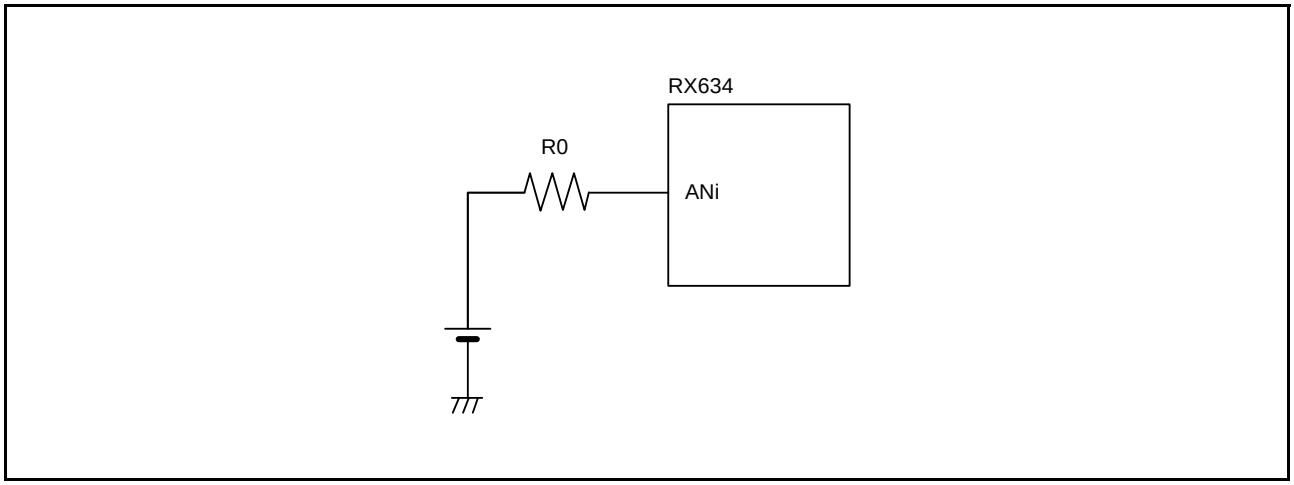


Figure 5.36 Internal Equivalent Circuit of Analog Input Pin

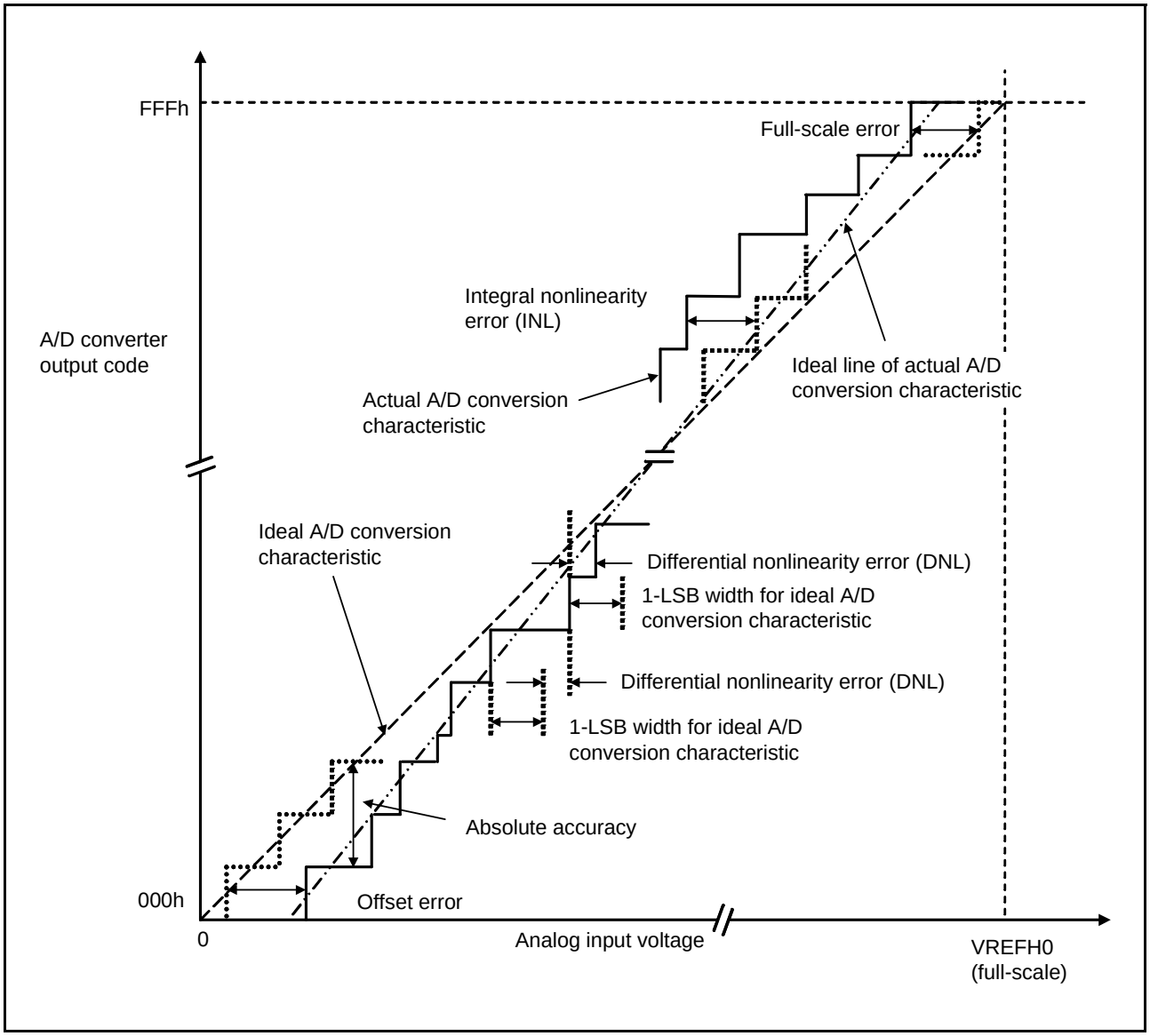


Figure 5.37 Illustration of A/D Converter Characteristic Terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and if reference voltage (VREFH0 = 5.12 V), then 1-LSB width becomes 1.25 mV, and 0 mV, 1.25 mV, 2.5 mV, ... are used as analog input voltages.

If analog input voltage is 10 mV, absolute accuracy = ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh though an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actually output code.

Offset error

Offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

5.5 D/A Conversion Characteristics

Table 5.33 D/A Conversion Characteristics (1)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	10	Bit	
Conversion time	—	—	±3.0	µs	20-pF capacitive load
Absolute accuracy	—	±3.0	±5.0	LSB	4-MΩ resistive load
	—	—	±4.0	LSB	8-MΩ resistive load
RO output resistance	—	3.6	—	kΩ	

5.6 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 5.34 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (1)

Conditions: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	2.46	2.58	2.7	V	Figure 5.38
	Voltage detection circuit (LVD0)	V_{DET0}	2.7	2.82	2.94		Figure 5.39
	Voltage detection circuit (LVD1)*1	V_{DET1_8}	2.75	2.90	3.05		Figure 5.40
		V_{DET1_9}	2.70	2.85	3.00		
		V_{DET1_A}	2.73	2.88	3.03		
	Voltage detection circuit (LVD2)*2	V_{DET2_8}	2.75	2.90	3.05		Figure 5.41
		V_{DET2_9}	2.70	2.85	3.00		
		V_{DET2_A}	2.73	2.88	3.03		
Internal reset time	Power-on reset (POR)	t_{POR}		9.7		ms	Figure 5.38
	Voltage detection circuit (LVD0)	t_{LVO0}		9.7			Figure 5.39
	Voltage detection circuit (LVD1)	t_{LVO1}		0.9			Figure 5.40
	Voltage detection circuit (LVD2)	t_{LVO2}		0.9			Figure 5.41
Minimum VCC down time*3		t_{VOFF}	200	—	—	µs	Figure 5.39 to Figure 5.41
Response delay time		t_{DET}			200	µs	
LVD operation stabilization time (after LVD is enabled)		$Td_{(E-A)}$			3	µs	Figure 5.40, Figure 5.41
Hysteresis width (LVD1 and LVD2)		V_{LVH}		80		mV	

Note 1. # in the symbol $V_{DET1\_\#}$ denotes the value of the LVDLVLR.LVD1LVL[3:0] bits.
Note 2. # in the symbol $V_{DET2\_\#}$ denotes the value of the LVDLVLR.LVD2LVL[3:0] bits.
Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{DET1}, and V_{DET2} for the POR/LVD.

Table 5.35 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (2)

Conditions: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	3.6	3.8	4.0	V	Figure 5.38
	Voltage detection circuit (LVD0)	V_{DET0}	4.0	4.2	4.4		Figure 5.39
	Voltage detection circuit (LVD1)*1	V_{DET1_8}	4.59	4.77	4.95		Figure 5.40
		V_{DET1_9}	4.05	4.23	4.41		
		V_{DET1_A}	4.32	4.50	4.68		
	Voltage detection circuit (LVD2)*2	V_{DET2_8}	4.59	4.77	4.95		Figure 5.41
		V_{DET2_9}	4.05	4.23	4.41		
		V_{DET2_A}	4.32	4.50	4.68		
Internal reset time	Power-on reset (POR)	t_{POR}		9.7		ms	Figure 5.38
	Voltage detection circuit (LVD0)	t_{LVO0}		9.7			Figure 5.39
	Voltage detection circuit (LVD1)	t_{LVO1}		0.9			Figure 5.40
	Voltage detection circuit (LVD2)	t_{LVO2}		0.9			Figure 5.41
Minimum VCC down time*3		t_{VOFF}	200	—	—	µs	Figure 5.39 to Figure 5.43
Response delay time		t_{DET}			200	µs	
LVD operation stabilization time (after LVD is enabled)		$Td_{(E-A)}$			3	µs	Figure 5.40, Figure 5.41
Hysteresis width (LVD1 and LVD2)		V_{LVH}		80		mV	

Note 1. # in the symbol $V_{DET1\_\#}$ denotes the value of the LVDLVLR.LVD1LVL[3:0] bits.
Note 2. # in the symbol $V_{DET2\_\#}$ denotes the value of the LVDLVLR.LVD2LVL[3:0] bits.
Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{DET1}, and V_{DET2} for the POR/LVD.

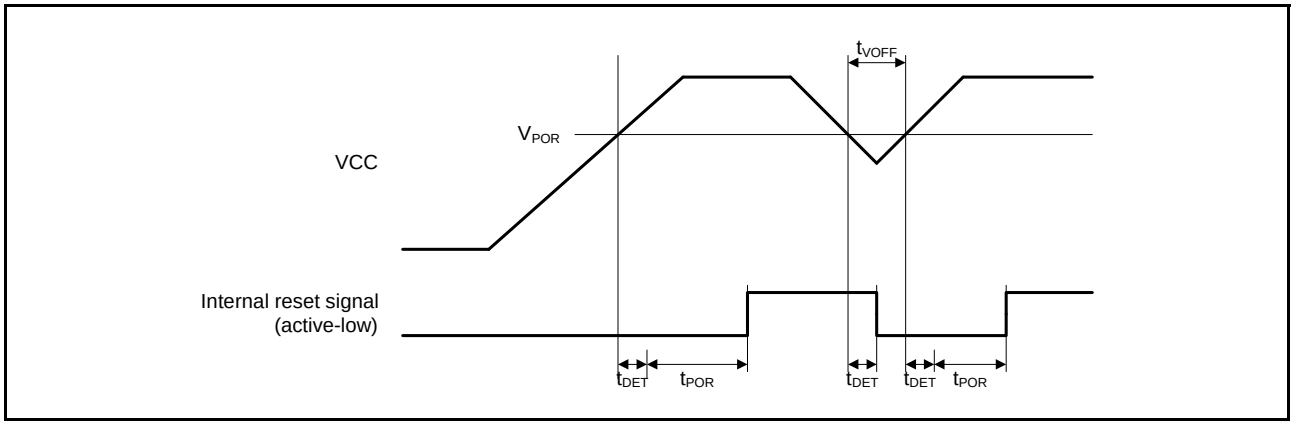


Figure 5.38 Power-on Reset Timing

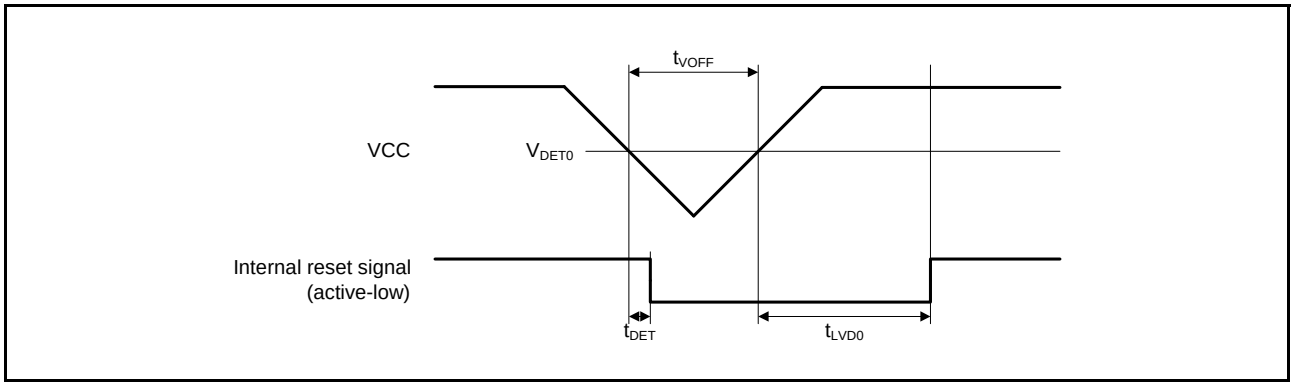


Figure 5.39 Voltage Detection Circuit Timing (V_{DET0})

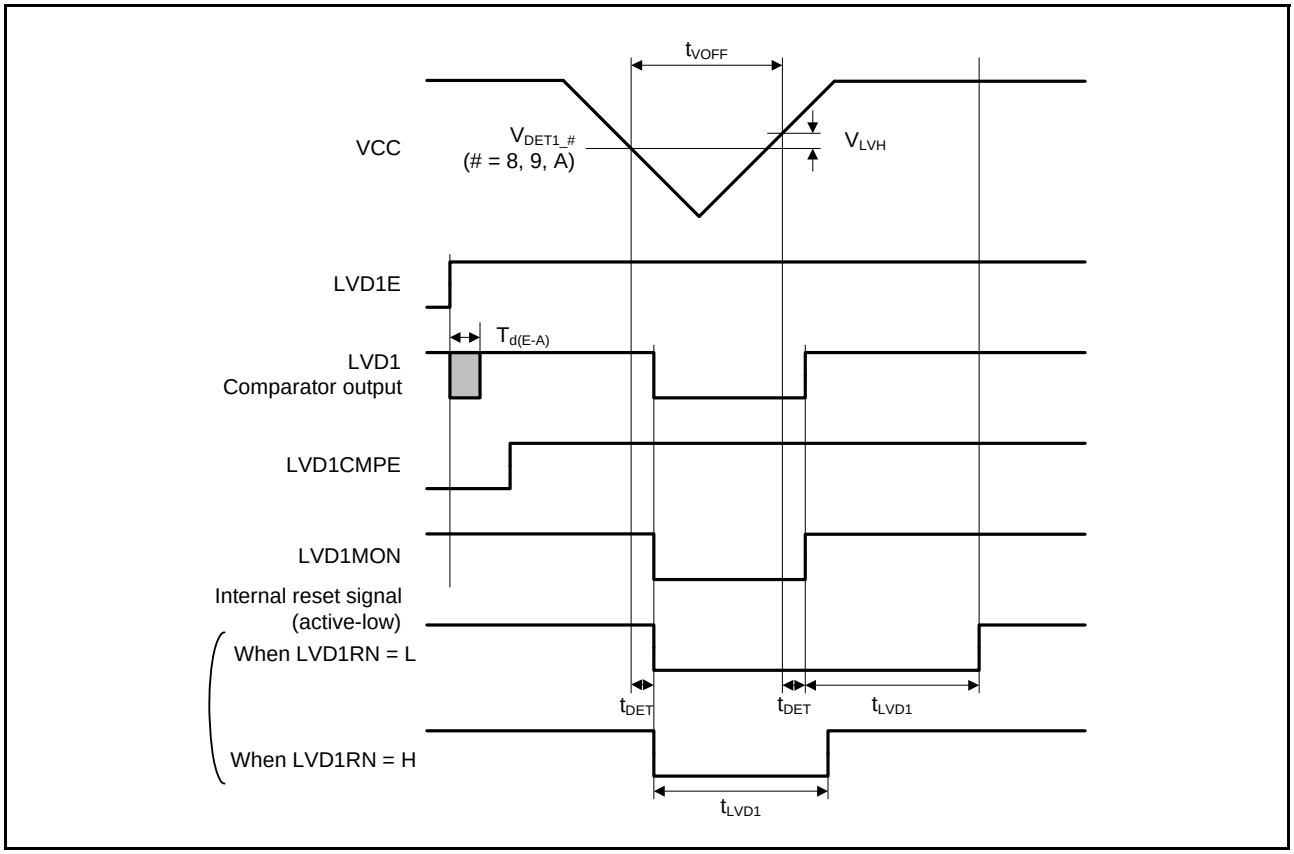


Figure 5.40 Voltage Detection Circuit Timing (V_{DET1})

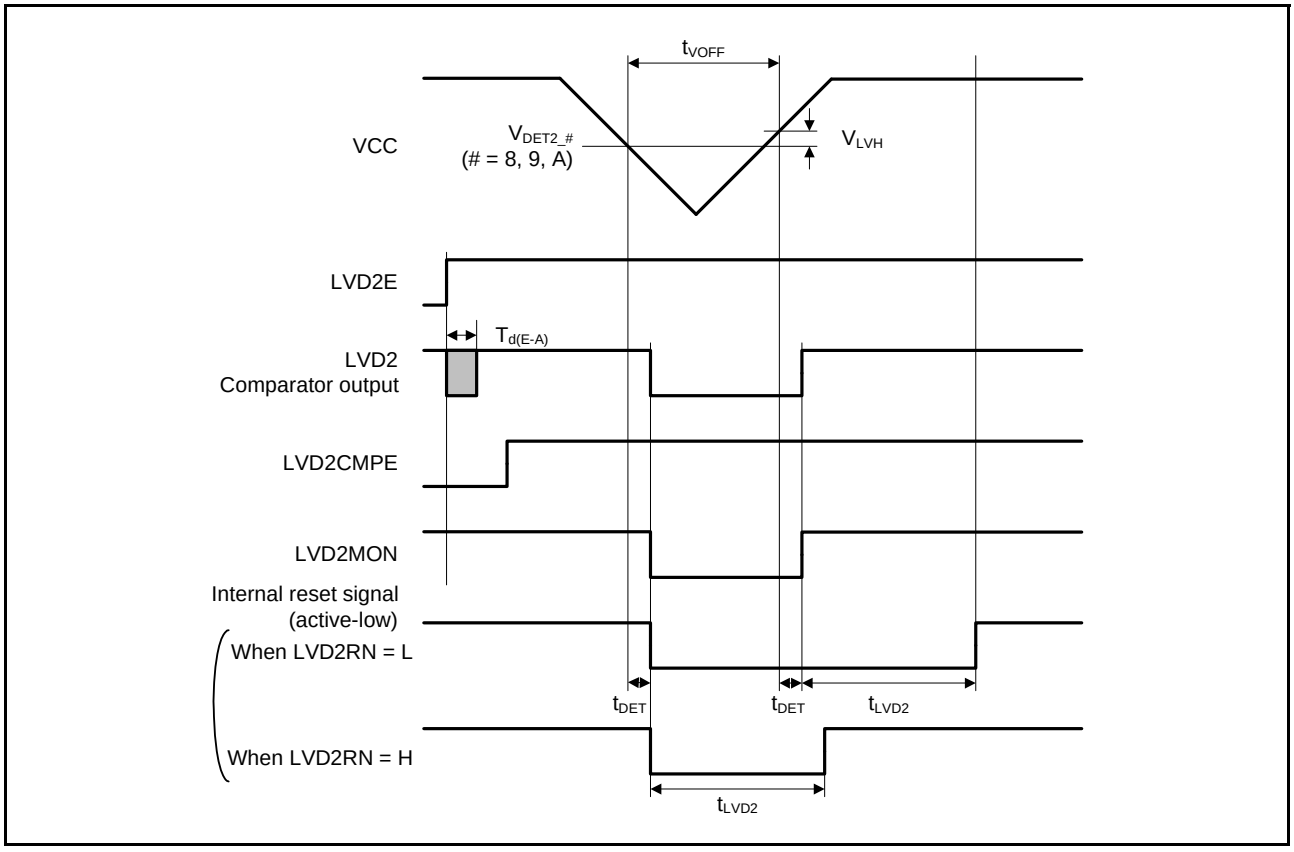


Figure 5.41 Voltage Detection Circuit Timing (V_{DET2})

5.7 Oscillation Stop Detection Timing

Table 5.36 Oscillation Stop Detection Circuit Characteristics

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 5.42

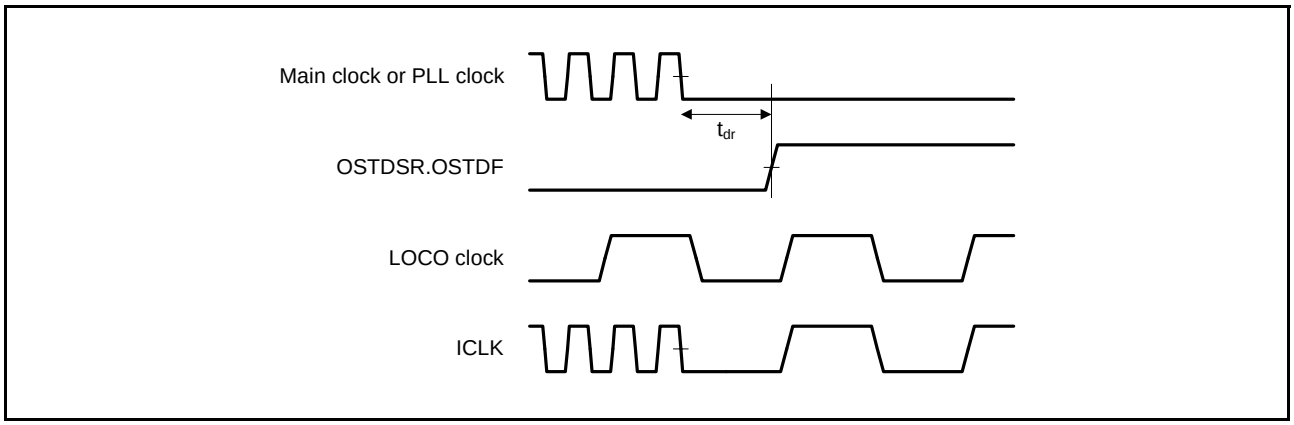


Figure 5.42 Oscillation Stop Detection Timing

5.8 ROM (Flash Memory for Code Storage) Characteristics

Table 5.37 ROM (Flash Memory for Code Storage) Characteristics (1)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +85°C T_a is common to both conditions 1 and 2.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reprogramming/erasure cycle*1	N_{pec}	1000	—	—	Times	
Data hold time	t_{DRP}	30*2	—	—	Year	T_a = +85°C

Note 1. Definition of reprogram/erase cycle: The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. This result is obtained from reliability testing.

Table 5.38 ROM (Flash Memory for Code Storage) Characteristics (2)

Note: The standard values of the items with no conditions specified in the table are common to conditions 1 and 2.
Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +85°C T_a is common to both conditions 1 and 2.

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{PEC} ≤ 100 times	128 bytes	t_{P128}	—	2.8	28	—	1	10	ms
	4 Kbytes	t_{P4K}	—	63	140	—	23	50	ms
	16 Kbytes	t_{P16K}	—	252	560	—	90	200	ms
Programming time when N_{PEC} > 100 times	128 bytes	t_{P128}	—	3.4	33.6	—	1.2	12	ms
	4 Kbytes	t_{P4K}	—	75.6	168	—	27.6	60	ms
	16 Kbytes	t_{P16K}	—	302.4	672	—	108	240	ms
Erasure time when N_{PEC} ≤ 100 times	4 Kbytes	t_{E4K}	—	50	120	—	25	60	ms
	16 Kbytes	t_{E16K}	—	200	480	—	100	240	ms
Erasure time when N_{PEC} > 100 times	4 Kbytes	t_{E4K}	—	60	144	—	30	72	ms
	16 Kbytes	t_{E16K}	—	240	576	—	120	288	ms
Suspend delay time during programming		t_{SPD}	—	—	400	—	—	120	µs
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	300	—	—	120	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	1.7	—	—	1.7	ms
Suspend delay time during erasing (in erasure priority mode)		t_{SEED}	—	—	1.7	—	—	1.7	ms
FCU reset time		t_{FCUR}	35	—	—	35	—	—	µs

5.9 E2 DataFlash (Flash Memory for Code Storage) Characteristics

Table 5.39 E2 DataFlash Characteristics (1)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +85°C T_a is common to both conditions 1 and 2.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reprogramming/erasure cycle*1	N_{DPEC}	100000	—	—	Times	
Data hold time	t_{DDRP}	30*2	—	—	Year	T_a = +85°C

Note 1. The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 8-byte programming is performed 16 times for different addresses in 128-byte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. This result is obtained from reliability testing.

Table 5.40 E2 DataFlash Characteristics (2)

Note: The standard values of the items with no conditions specified in the table are common to conditions 1 and 2.
Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6V, VREFH = 2.7V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0V
Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5V, VREFH = 4.0V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0V
Temperature range for the programming/erasure operation: T_a = –40 to +85°C T_a is common to both conditions 1 and 2.

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{PEC} ≤ 100 times	2 bytes	t_{DP2}	—	0.7	6	—	0.25	2	ms
Programming time when N_{PEC} > 100 times	2 bytes	t_{DP2}	—	0.7	6	—	0.25	2	ms
Erasure time when N_{PEC} ≤ 100 times	32 bytes	t_{DE32}	—	4	40	—	2	20	ms
Erasure time when N_{PEC} > 100 times	32 bytes	t_{DE32}	—	7	40	—	4	20	ms
Blank check time	2 bytes	t_{DBC2}	—	—	100	—	—	30	µs
Suspend delay time during programming		t_{DSPD}	—	—	250	—	—	120	µs
First suspend delay time during erasing (in suspend priority mode)		t_{DSESD1}	—	—	250	—	—	120	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{DSESD2}	—	—	500	—	—	300	µs
Suspend delay time during erasing (in erasure priority mode)		t_{DSEED}	—	—	500	—	—	300	µs

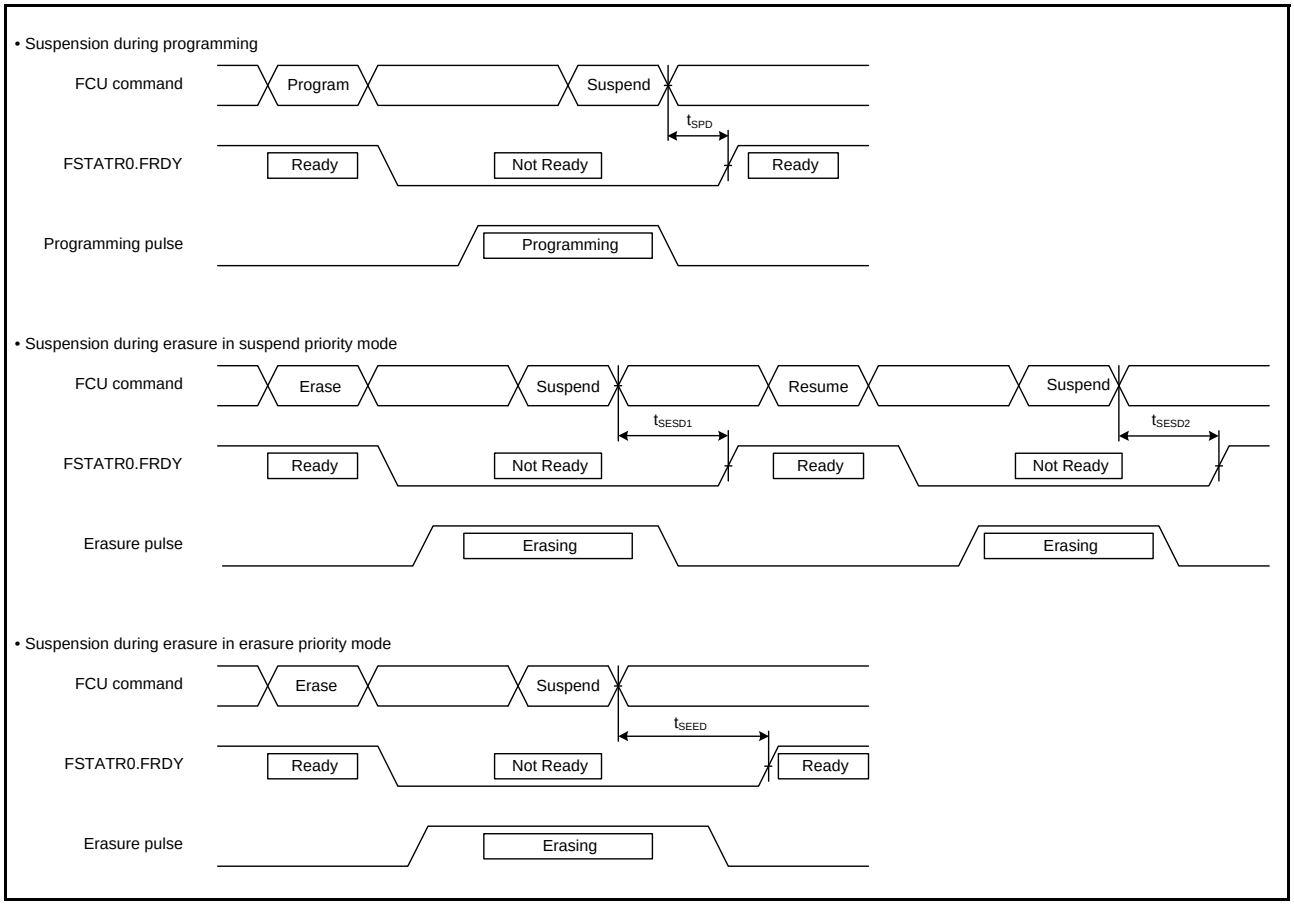
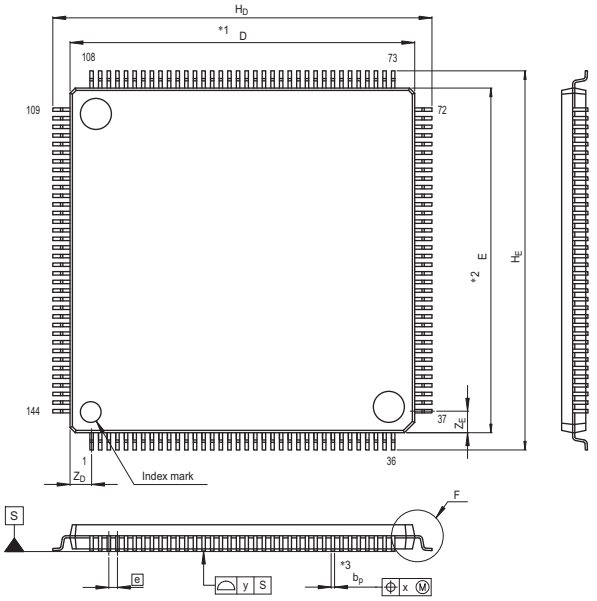


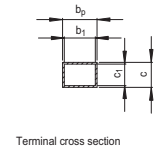
Figure 5.43 Flash Memory Program/Erase Suspend Timing

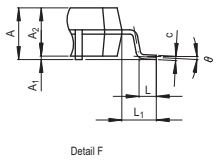
Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP144-20x20-0.50	PLQP0144KA-A	144P6Q-A / FP-144L / FP-144LV	1.2g







NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure A 144-Pin LQFP (PLQP0144KA-A)

REVISION HISTORY	RX634 Group Datasheet

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.00	Feb 25, 2014	—	First edition, issued	

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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